



NFORCE6M-A v : 2.0

SCHEMATICS TABLE:

Page	Index
1	COVER PAGE
2	BLOCK DIADRAM
3	BLOCK DISTRIBUTION
4	CPU M2-1 HyperTransport
5	CPU M2-1 DDR2
6	CPU M2-3 Miscellany
7	CPU M2-4 Power and Ground
8	DDR2 DIMM
9	DDR2 DIMM
10	DDR2 Termination
11	MCP61 HT
12	MCP61 PCI-E X16
13	MCP61 PCI-E X1/RGMII/DAC
14	MCP61 PCI
15	MCP61 SATA/ESATA/IDE

Page	Index
16	MCP61 AUDIO/USB/MISC
17	MCP61 PWR/GND
18	MCP61 DECOUPLING/SPI
19	PCIE LAN RTL8111B/RTL8111C/RTL8101E
20	PCI-E X16 CONN
21	PCI1/PCI2
22	PCI-E X1/TPM/PCI 3
23	W83627EHG/FDD
24	PS2/COM/LPT
25	USB
26	AUDIO 92HD202/206
27	AUDIO 92HD202/206(PANEL)
28	PWR CON/FNT PNL
29	CPU VCORE
30	DC-DC
31	ATTENTION

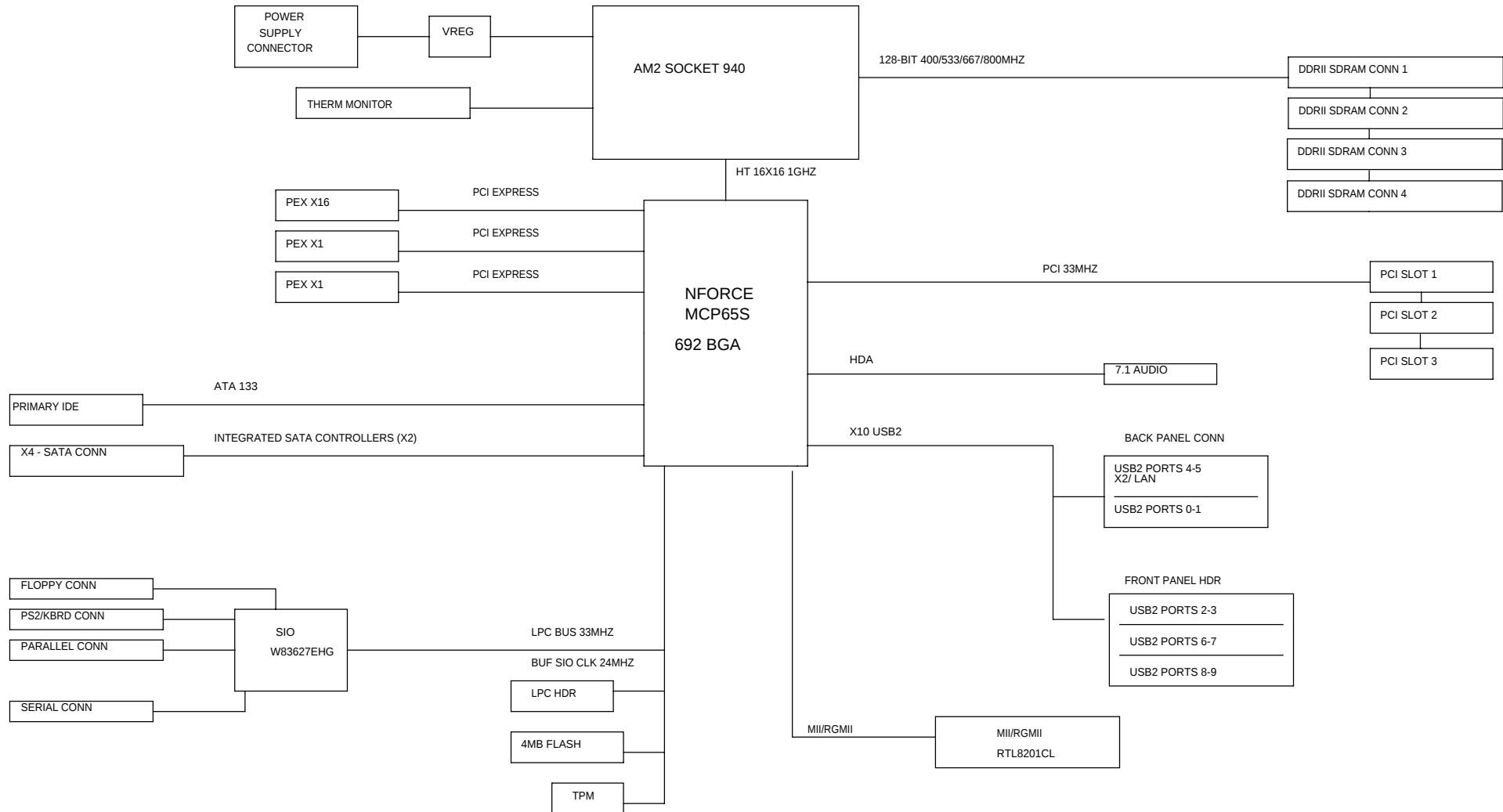
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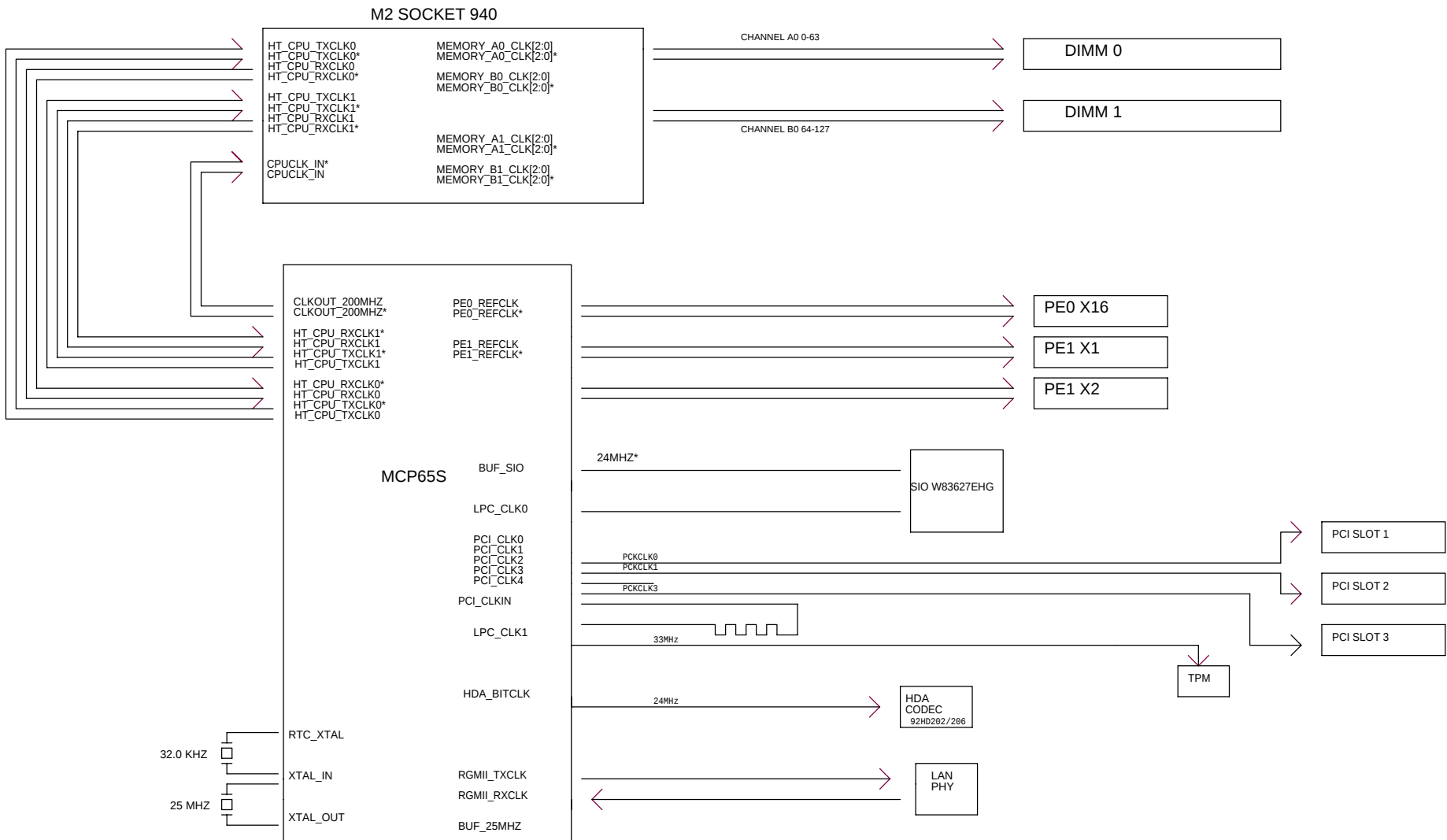
Rev	Date	Notes
A	01-23-2007	INITIAL RELEASE
1.0	02-26-2007	
2.0	04-27-2007	* Page13: Unused MII Interface; Pull PE2_PRST- to GND to support PCI-E LAN; * Page16: Set net AZ_RST- pull high/low selectable by RJ8; * Page19: Change PHY LAN to PCI-E Giga LAN; * Page22: Remove PCIEX2 to support PCI-E LAN; * Page23: Add net GP_RESERVE1 to detect the M/B's Version; * Page26: Change MC2 from 1U to 10U and change EC48 from 1U to 100U to reduce noise.

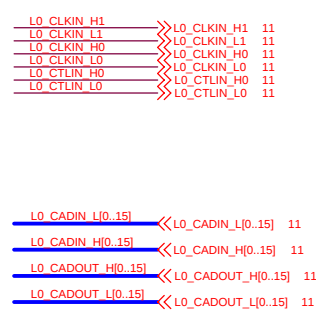
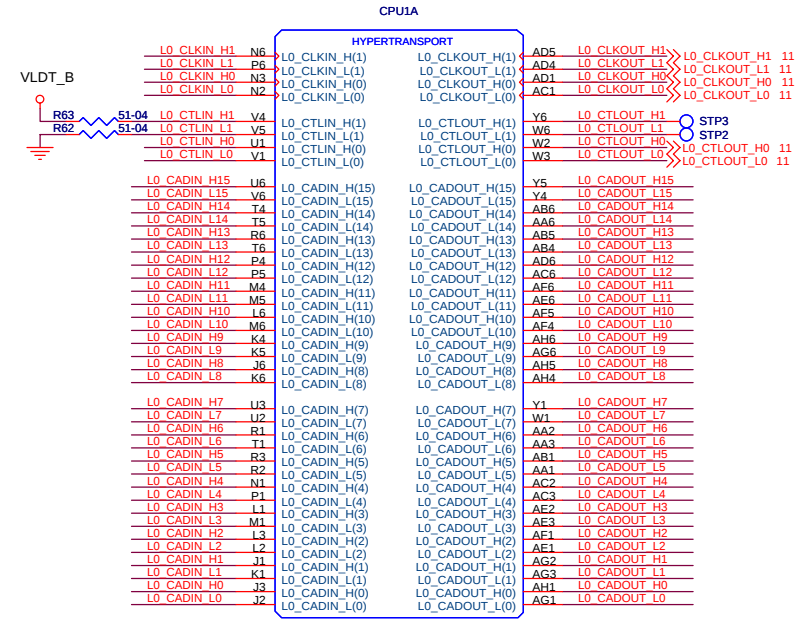
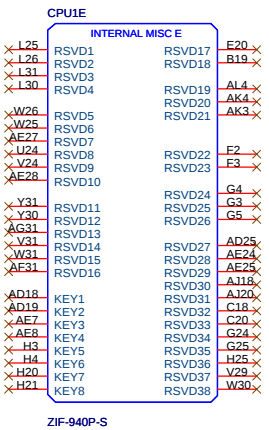
PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

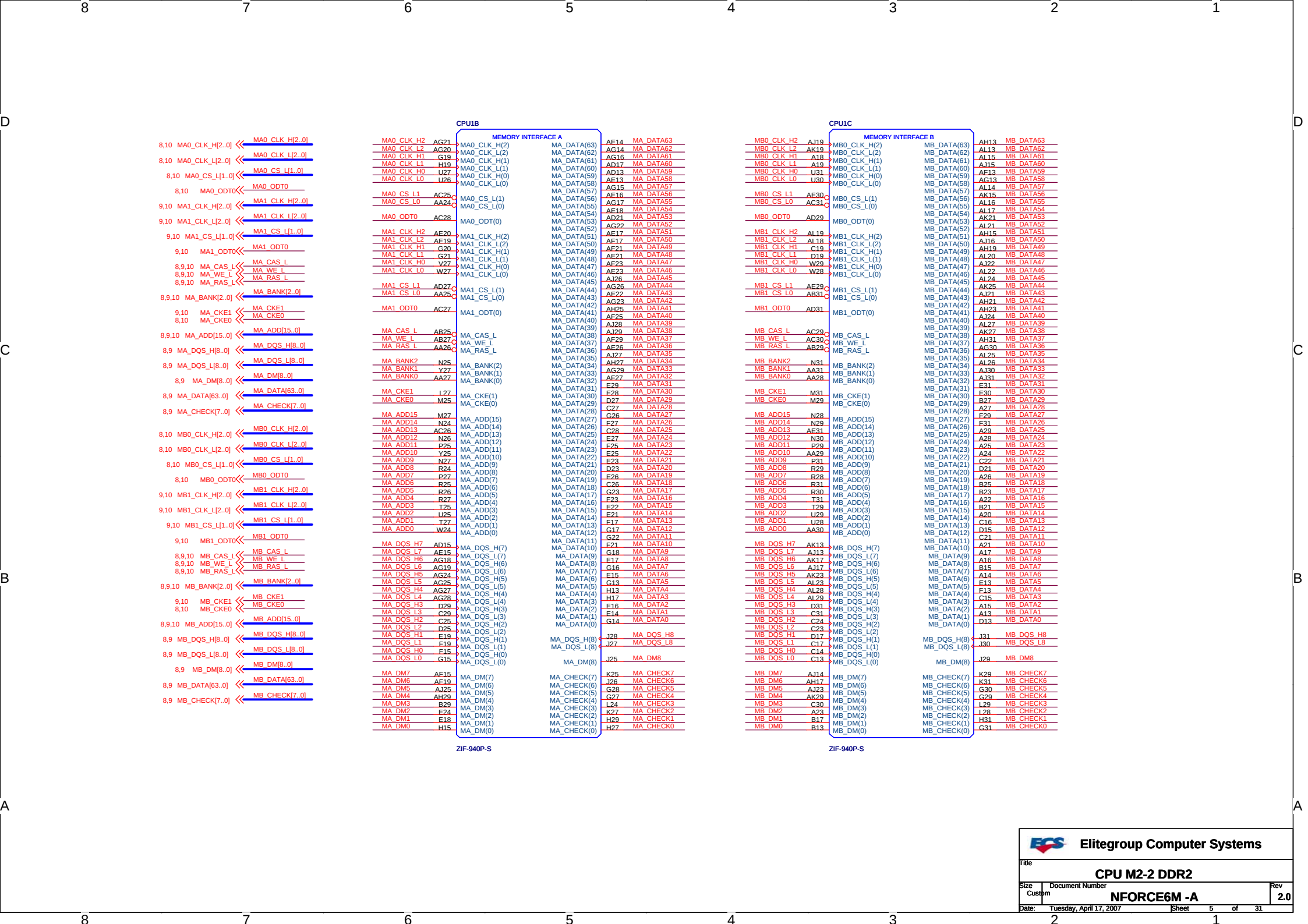
 Elitegroup Computer Systems	
Title Cover Page	
Size Custom	Document Number NFORCE6M-A Rev 2.0
Date: Monday, April 30, 2007	Sheet 1 of 31

BLOCK DIAGRAM





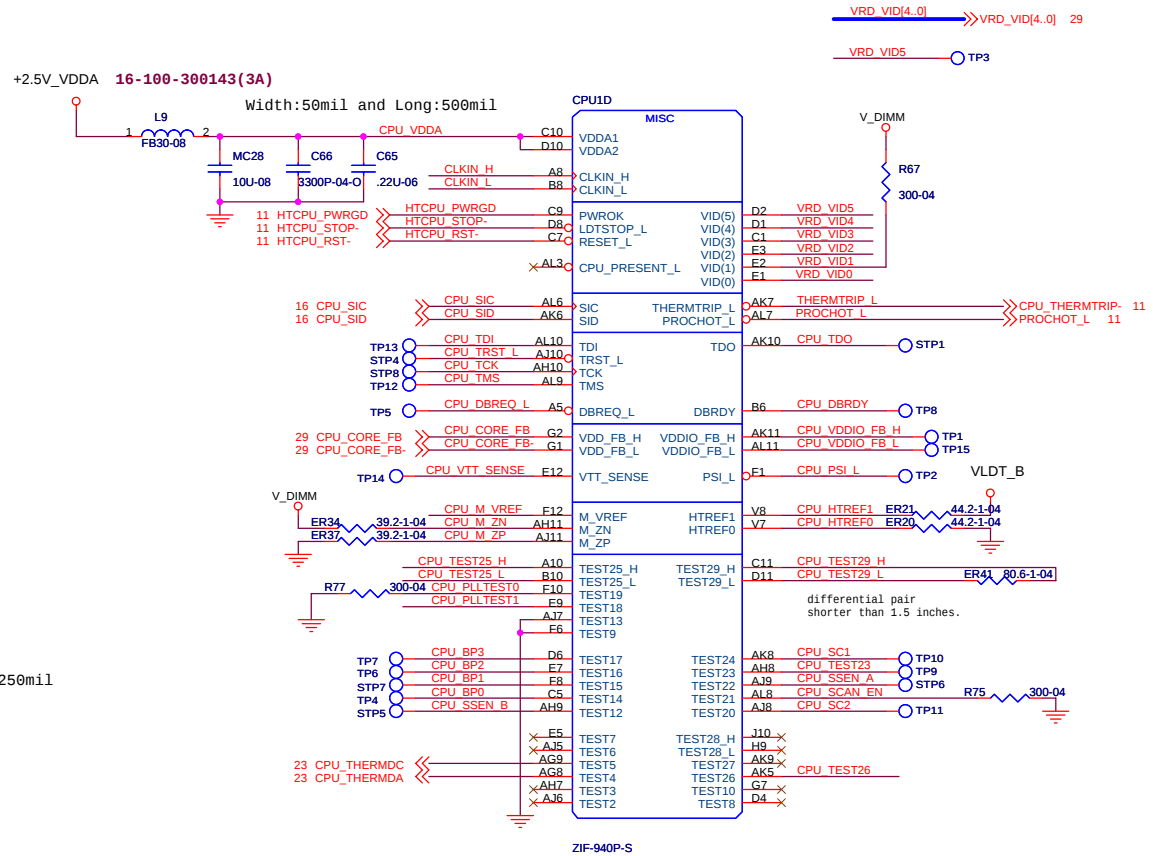
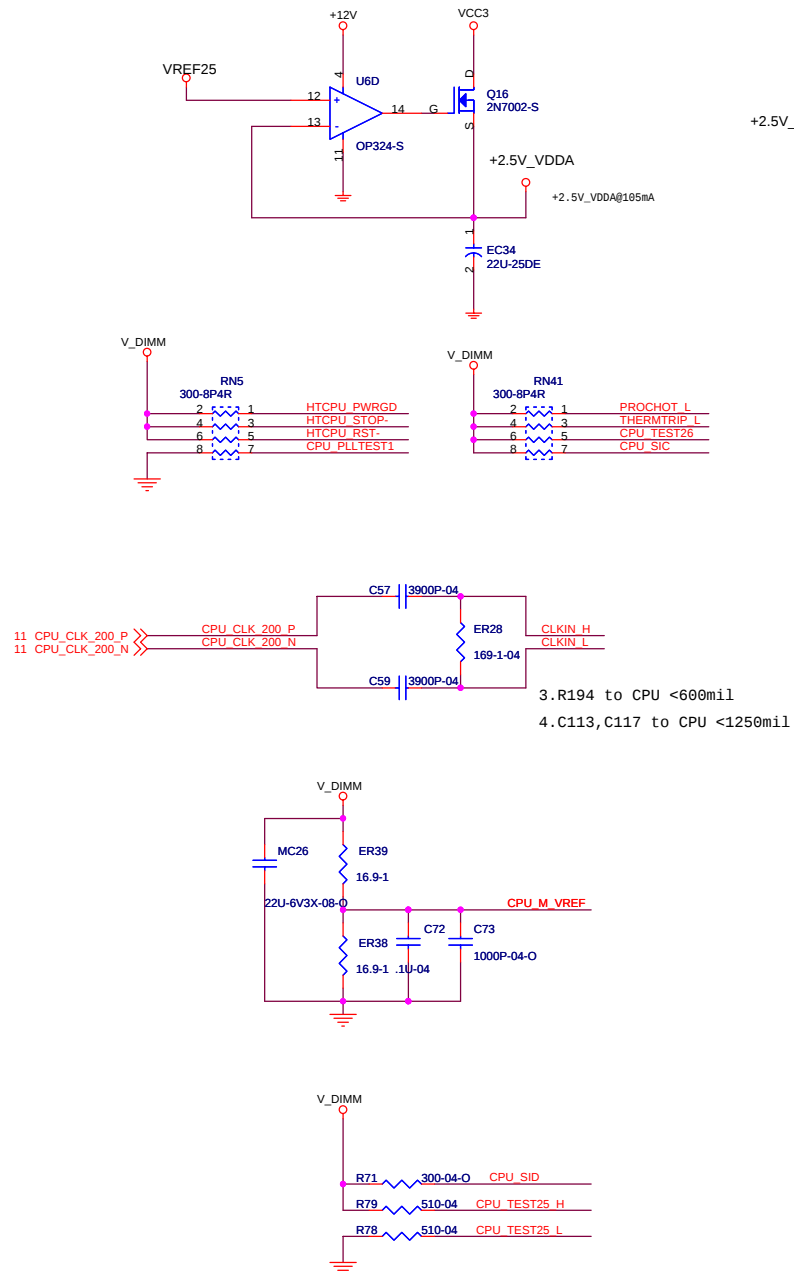


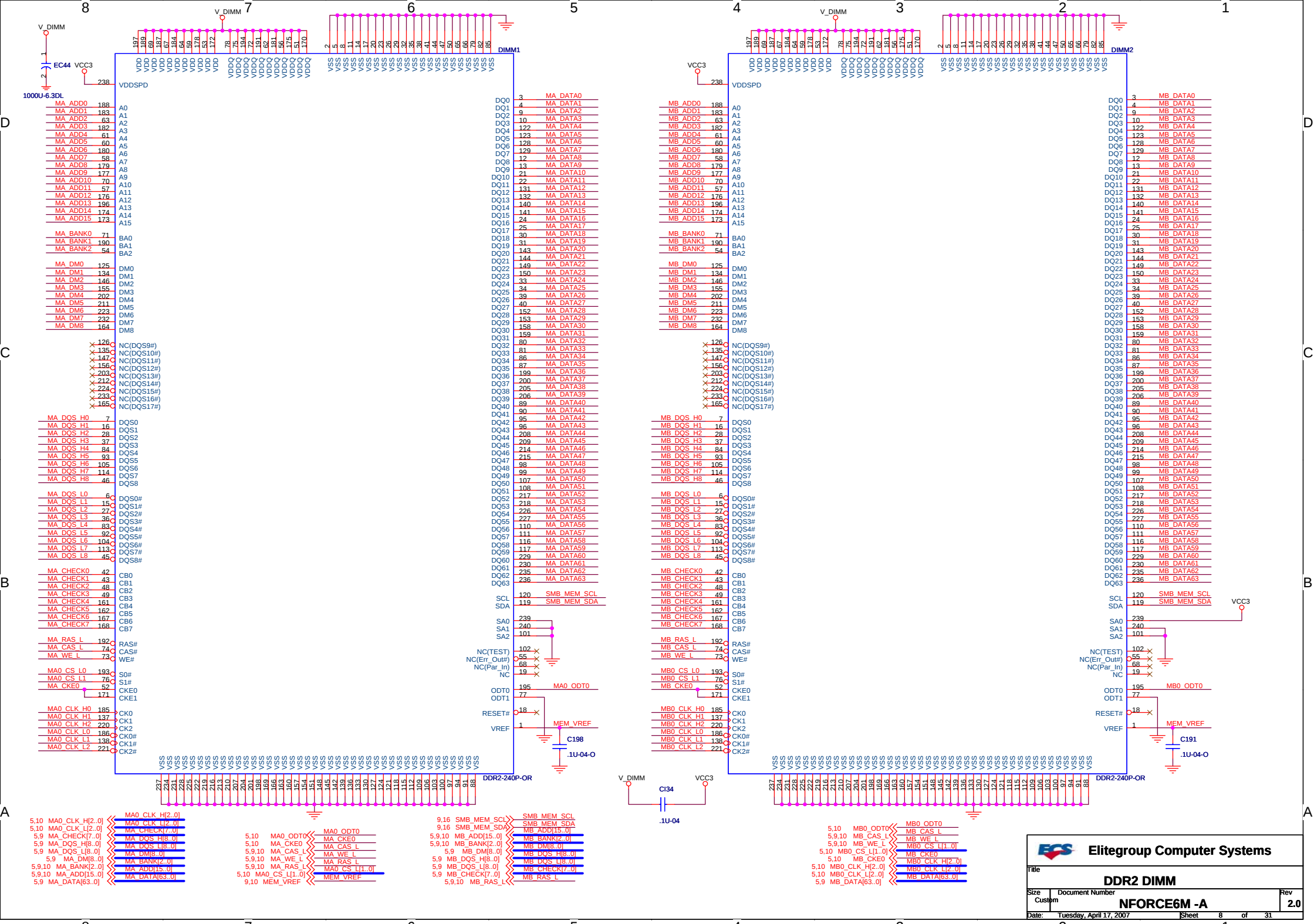


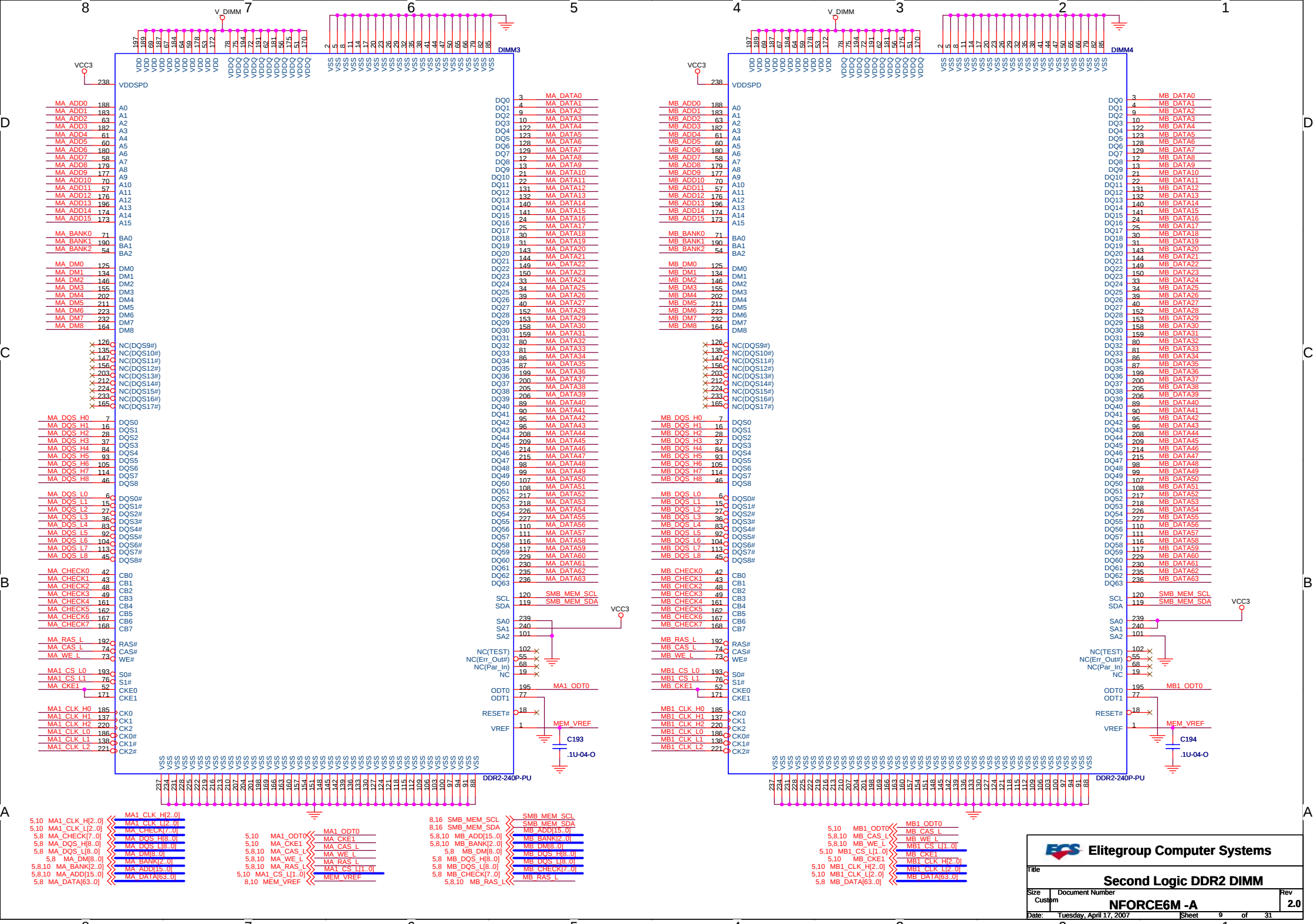
Elitegroup Computer Systems

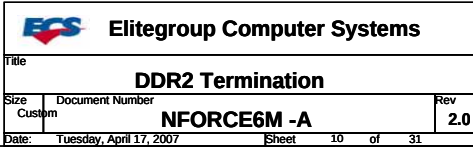
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Size			Document Number		
Custom			NFORCE6M -A		
Date:			Tuesday, April 17, 2007		
Sheet			5 of 31		
Rev			2.0		

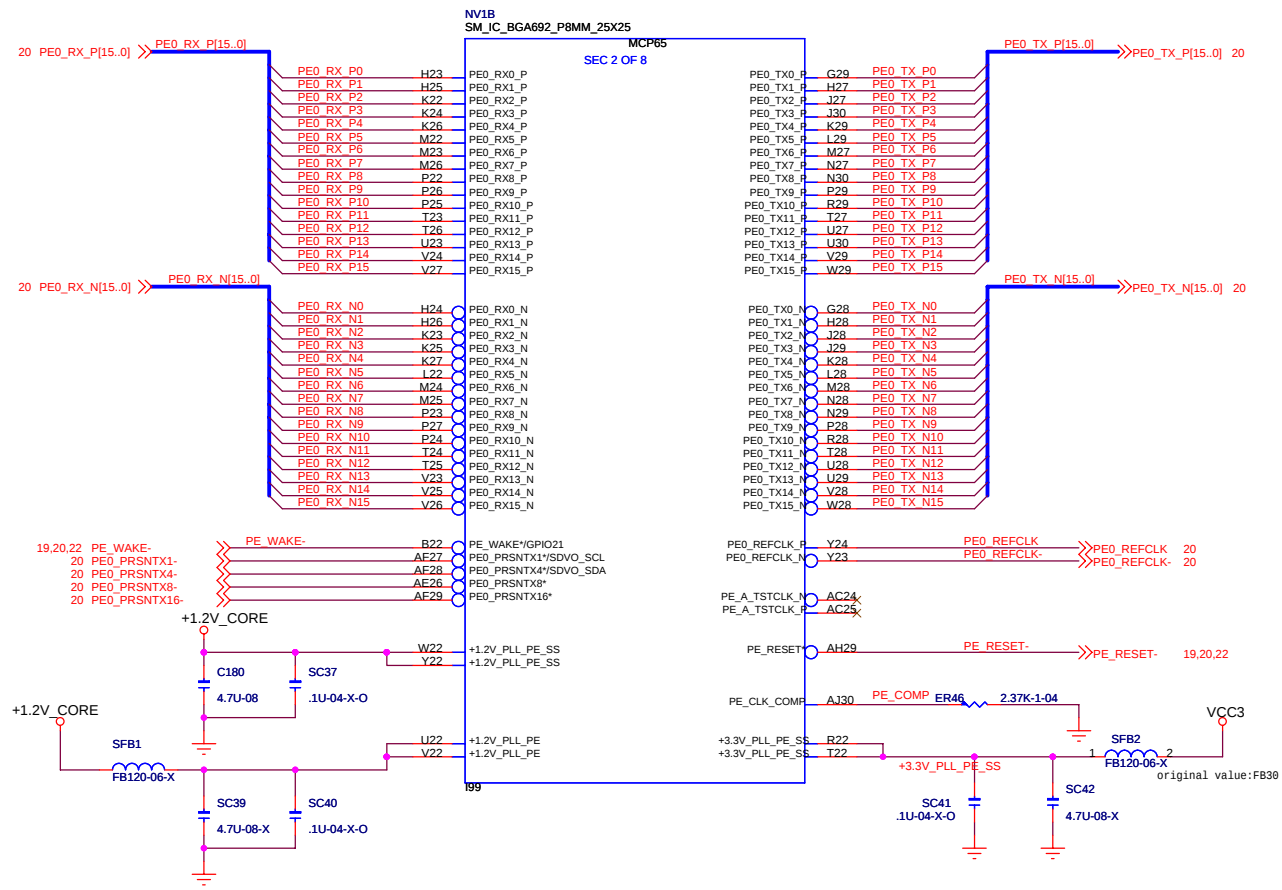
+2.5V_VDDA for CPU PLL

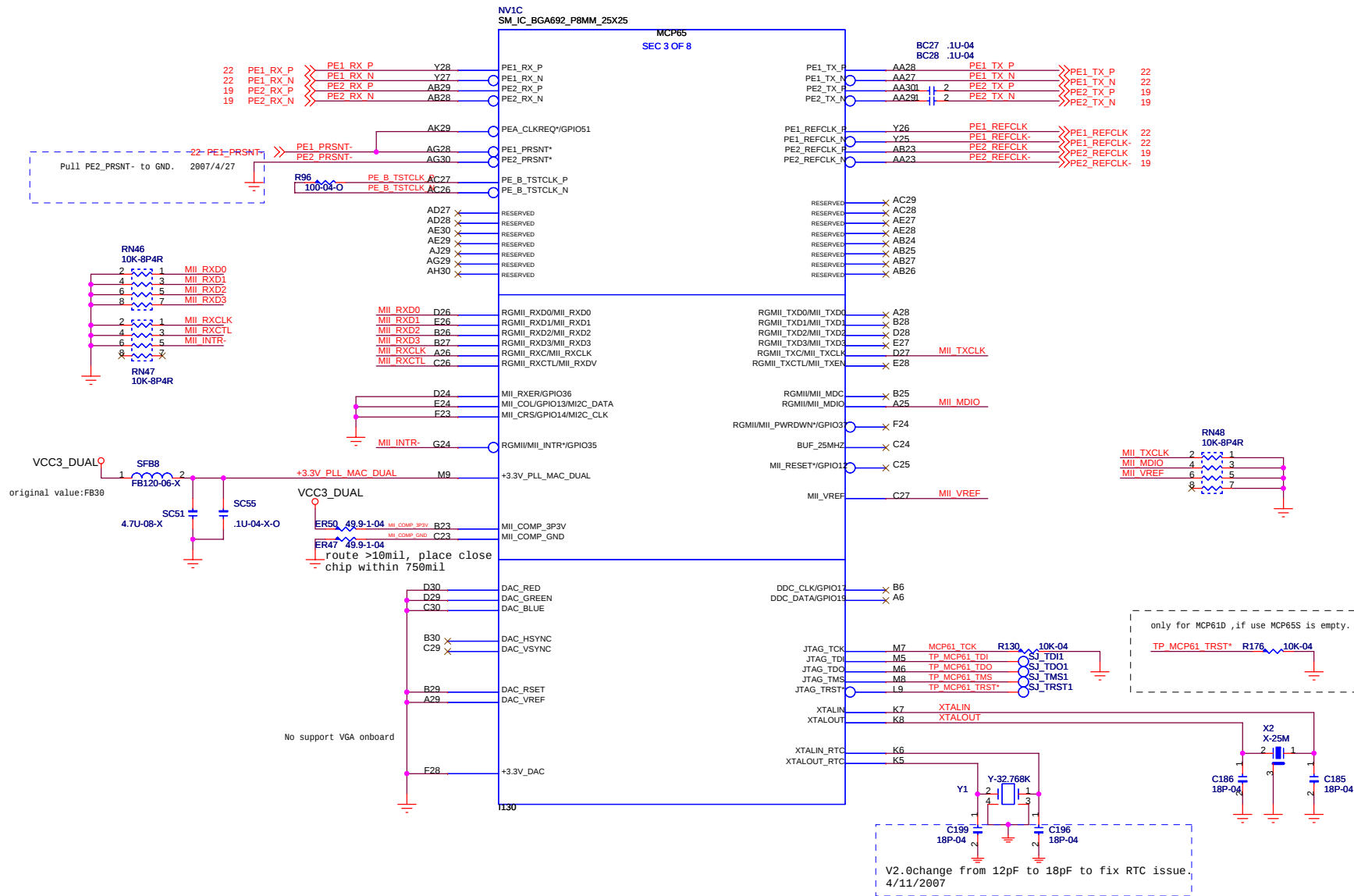


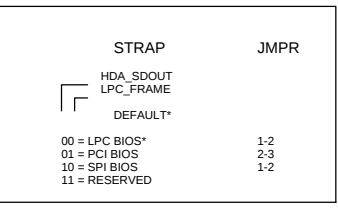
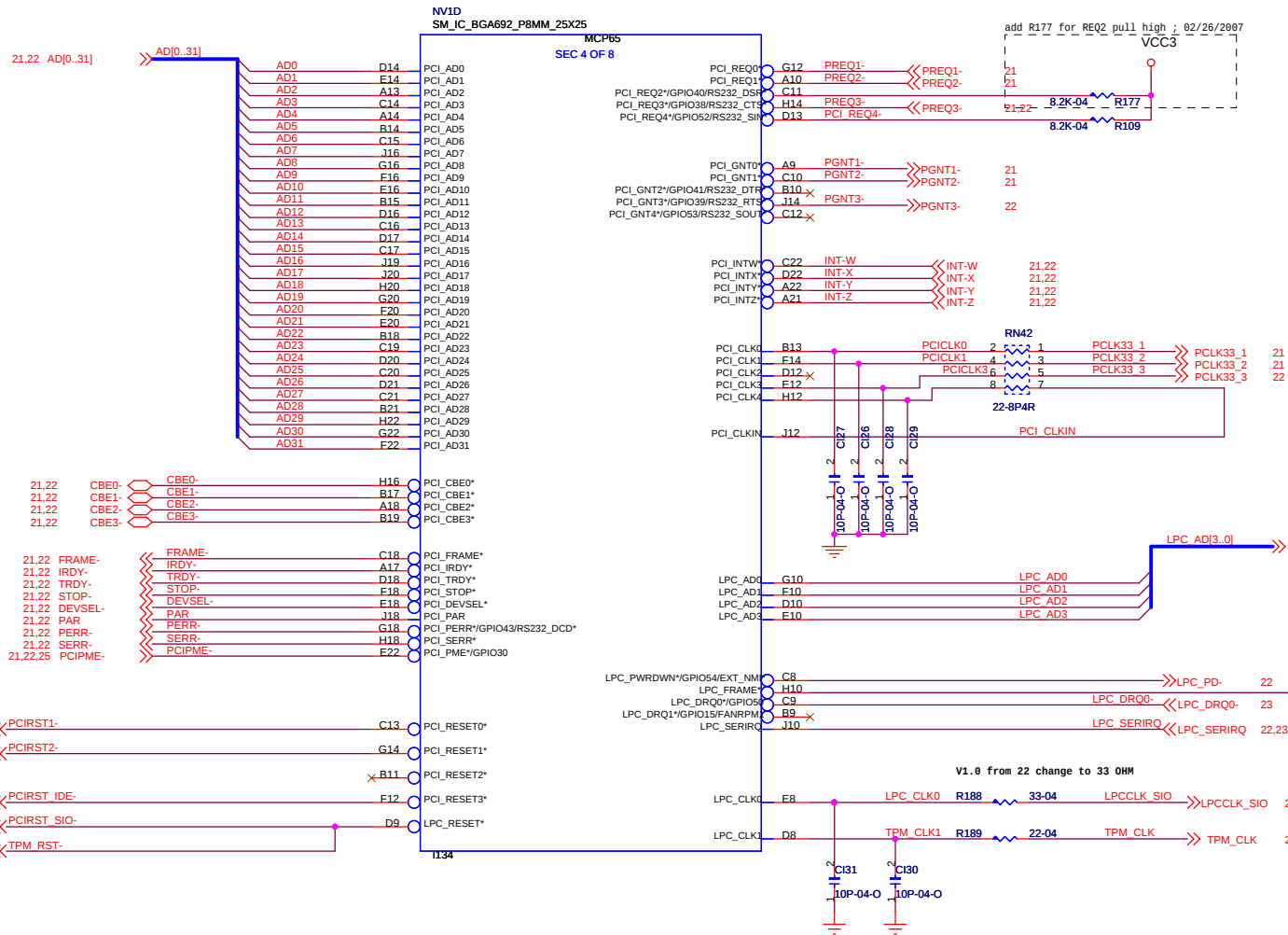


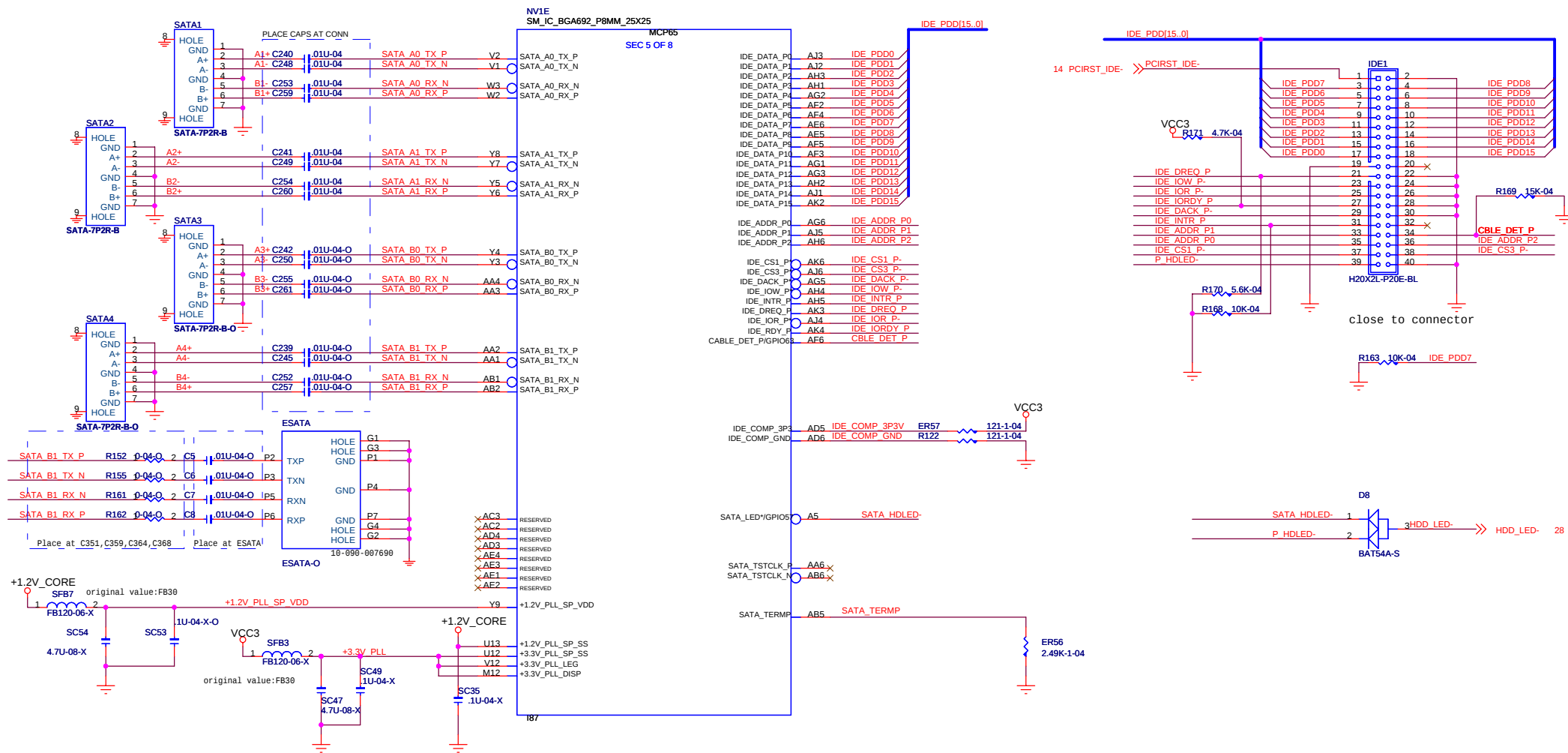












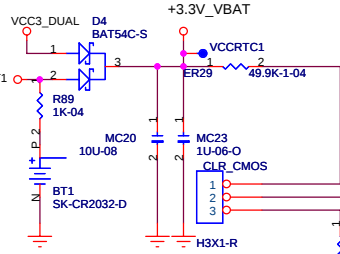
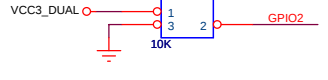
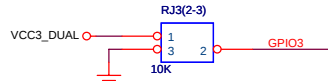
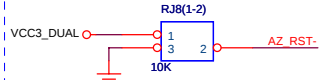
REMOVE FOR PRODUCTION

AC_RST*
1 = *RGMII
0 = MII

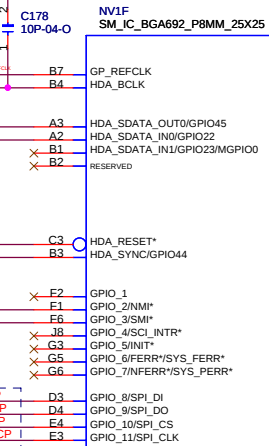
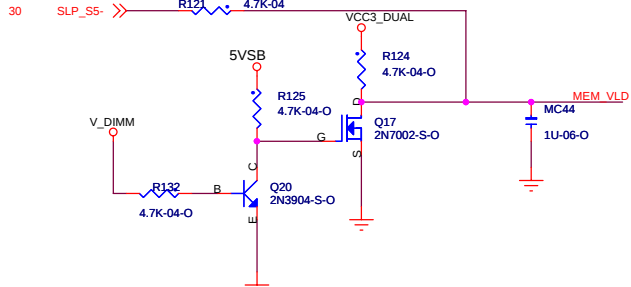
AC_SYNC
(SIO CLK)
1 = *24MHZ
0 = 14.318MHZ

* = DEFAULT

MCP65S need pull HDA_RESET- to VCC3_DUAL.
04/11/2007

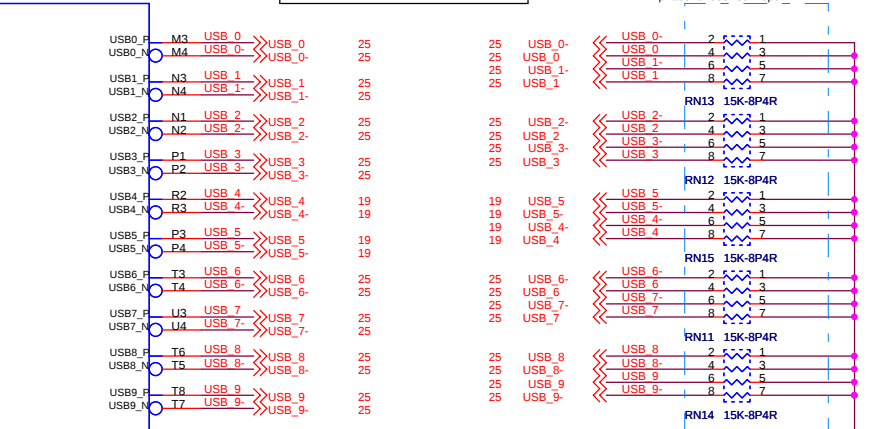


CLR_CMOS	CLEAR_CMOS
1-2	NORMAL
2-3	CLEAR

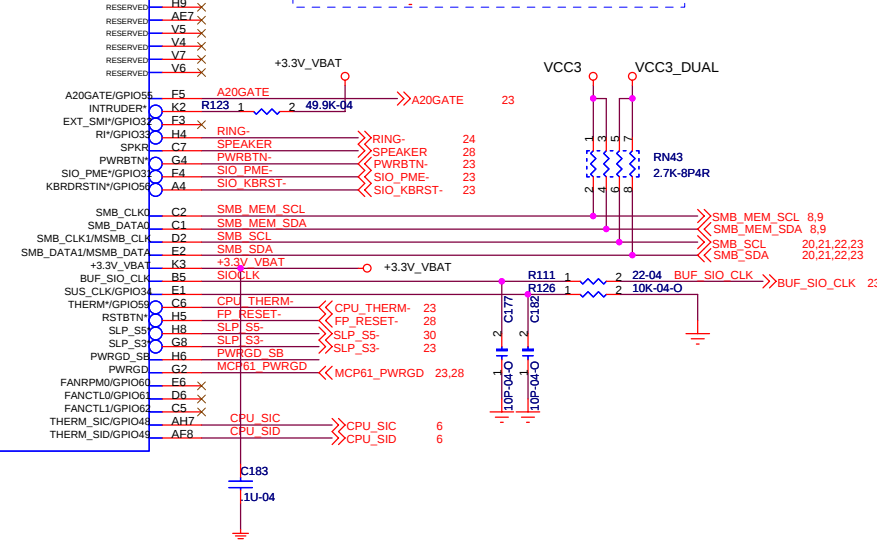


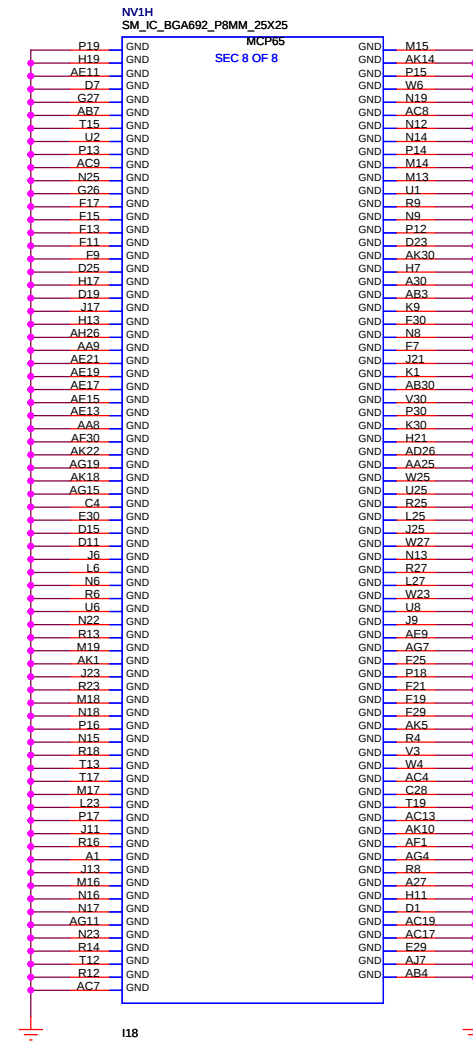
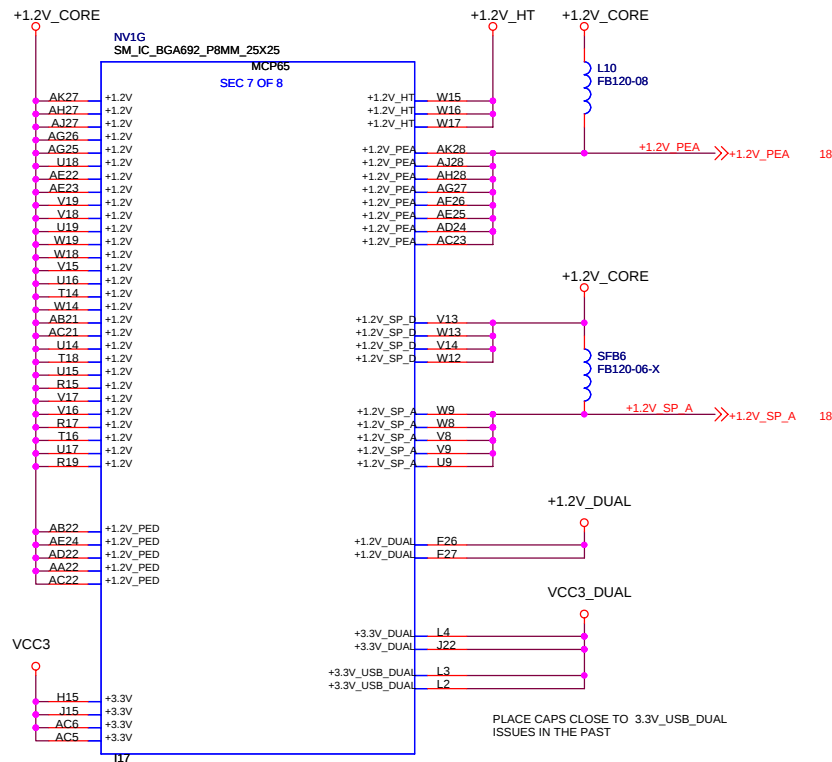
SEC 6 OF 8

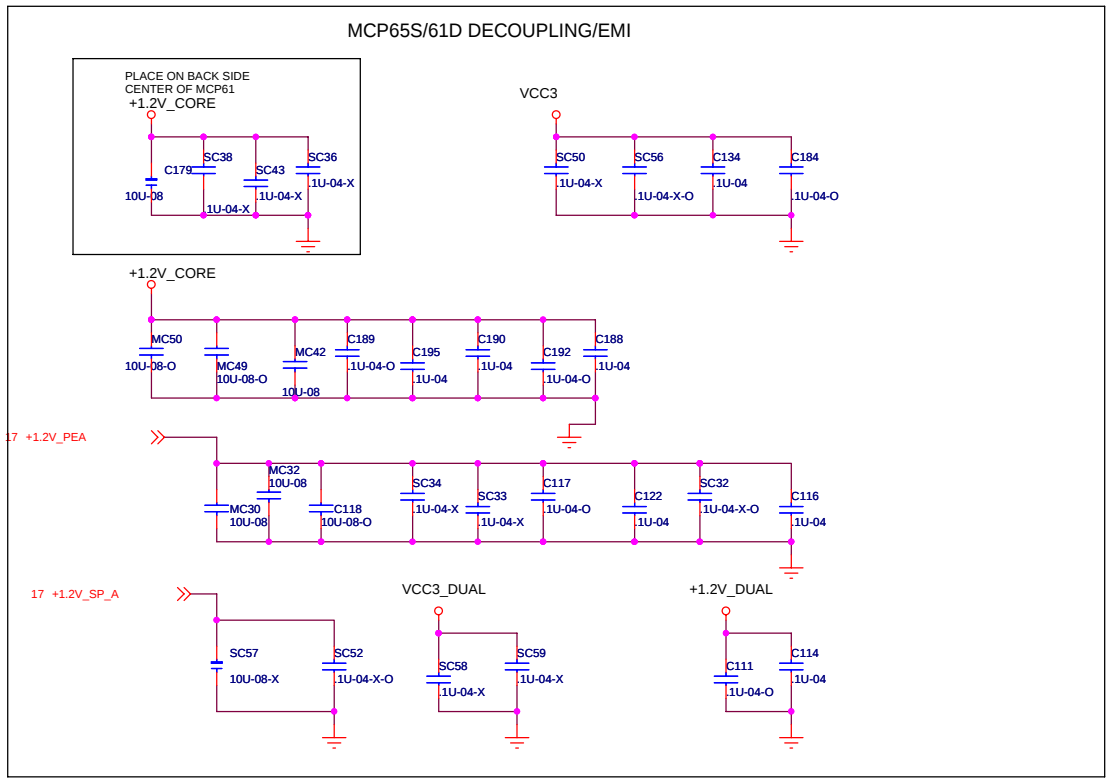
USB0,1,4,5 --> BACK CONNECTORS
USB2,3,7,6,7,8,9 --> ON-BOARD HEADER



V2.0 change to 931 OHM
04/11/2007



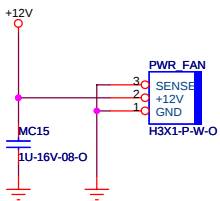




MCP65/61D INTERNAL PULL-UP/DOWN'S

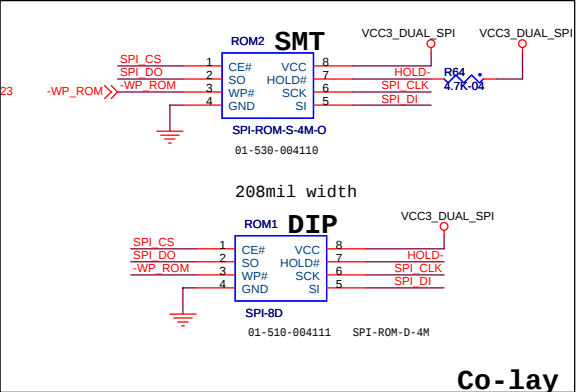
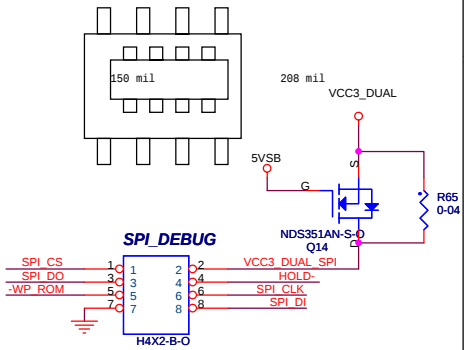
PE0_PRSENTX16*	10K PU TO 3.3V
PE0_PRSENTX8*	10K PU TO 3.3V
PE1_PRSENT*	10K PU TO 3.3V
PE2_PRSENT*	10K PU TO 3.3V
PE1_CLKREQ*	10K PU TO 3.3V
PCI_PME*/GPIO_30	8.2K PU TO 3.3V_DUAL
LPC_AD0	8.2K PU TO 3.3V
LPC_AD1	8.2K PU TO 3.3V
LPC_AD2	8.2K PU TO 3.3V
LPC_AD3	8.2K PU TO 3.3V
LPC_DRQ1/LPC_CS*	8.2K PU TO 3.3V
LPC_DRQ0*	8.2K PU TO 3.3V
LPC_SERIRQ	10K PU TO 3.3V
HDA_SDATA_IN1/GPIO_23/MGPIO_0	10K PD TO GND
HDA_SDATA_IN0/GPIO_22	10K PD TO GND
JTAG_TMS	10K PU TO 3.3V
JTAG_TRST*	10K PD TO GND
JTAG_TDI	10K PU TO 3.3V
A20GATE	10K PU TO 3.3V
PE_WAKE*	10K PU TO 3.3V_DUAL
EXT_SMI*/GPIO32	10K PU TO 3.3V_DUAL
THERM*/GPIO_59	10K PU TO 3.3V
KBRDRSTIN*/GPIO_58	10K PU TO 3.3V
RIP*/GPIO_33	10K PU TO 3.3V_DUAL
SIO_PME*/GPIO_31/MGPIO_2	10K PU TO 3.3V_DUAL
PWRBTN*	10K PU TO 3.3V_DUAL
RSTBTN*	10K PU TO 3.3V_DUAL

MCP61 FAN HDR



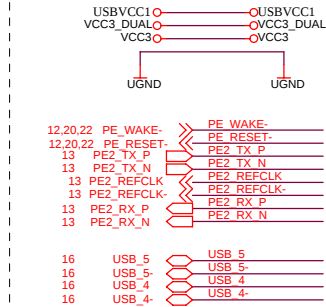
SPI_DO >>> SPI_DI_MCP 16
 SPI_DI <<< SPI_DO_MCP 16
 SPI_CLK <<< SPI_CLK_MCP 16
 SPI_CS <<< SPI_CS_MCP 16

S08 MN and MW co-layout layout draw



for SPI ROM

External Connection



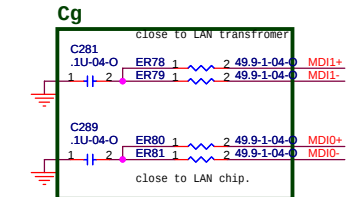
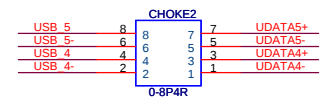
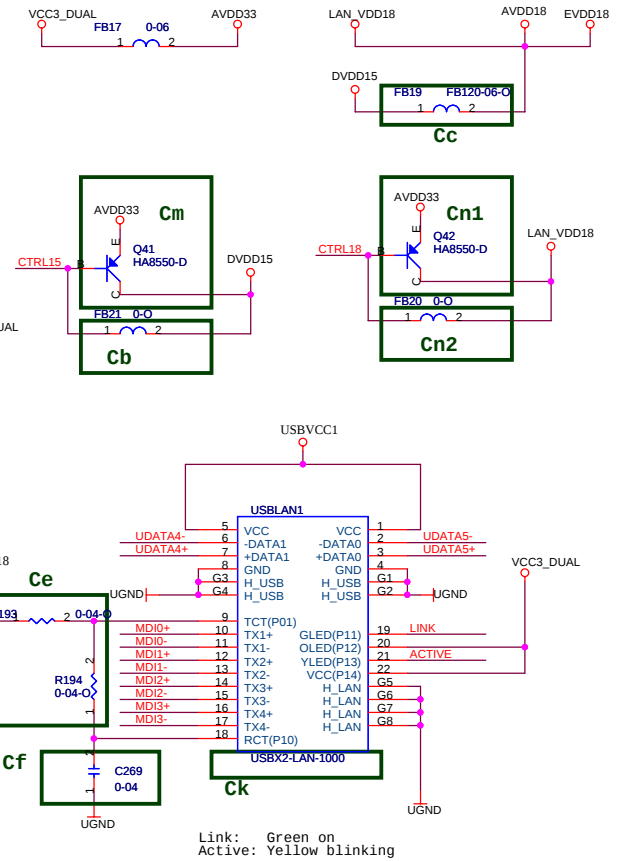
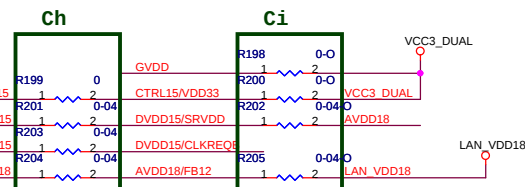
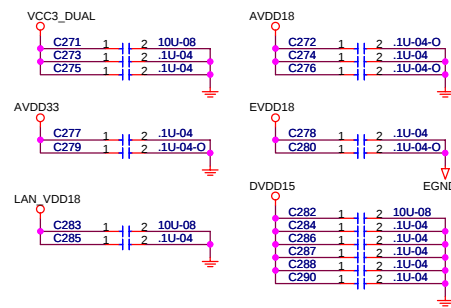
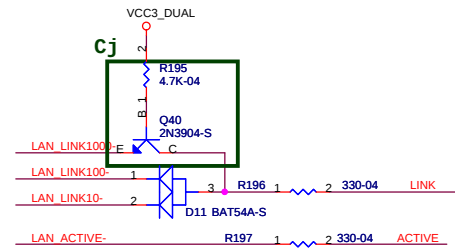
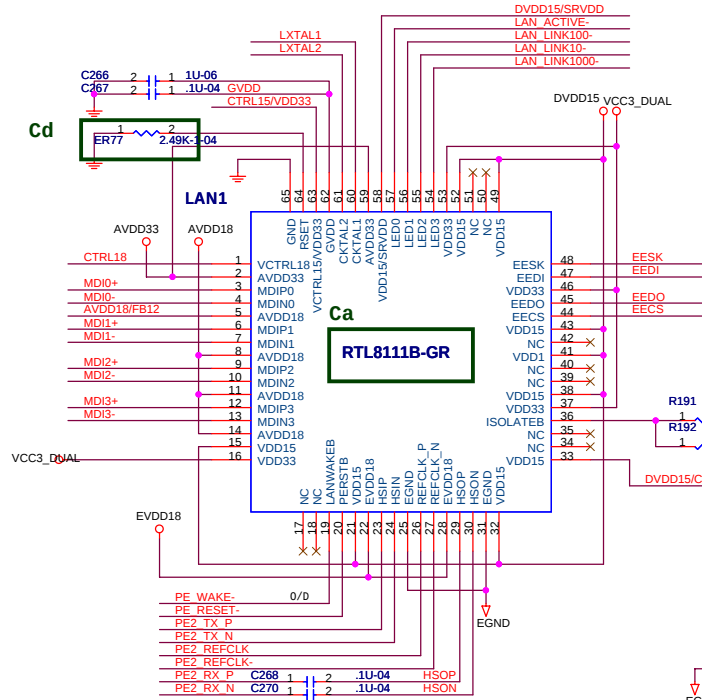
When you found some bug, please inform Ren(EXT:685) to update circuit.

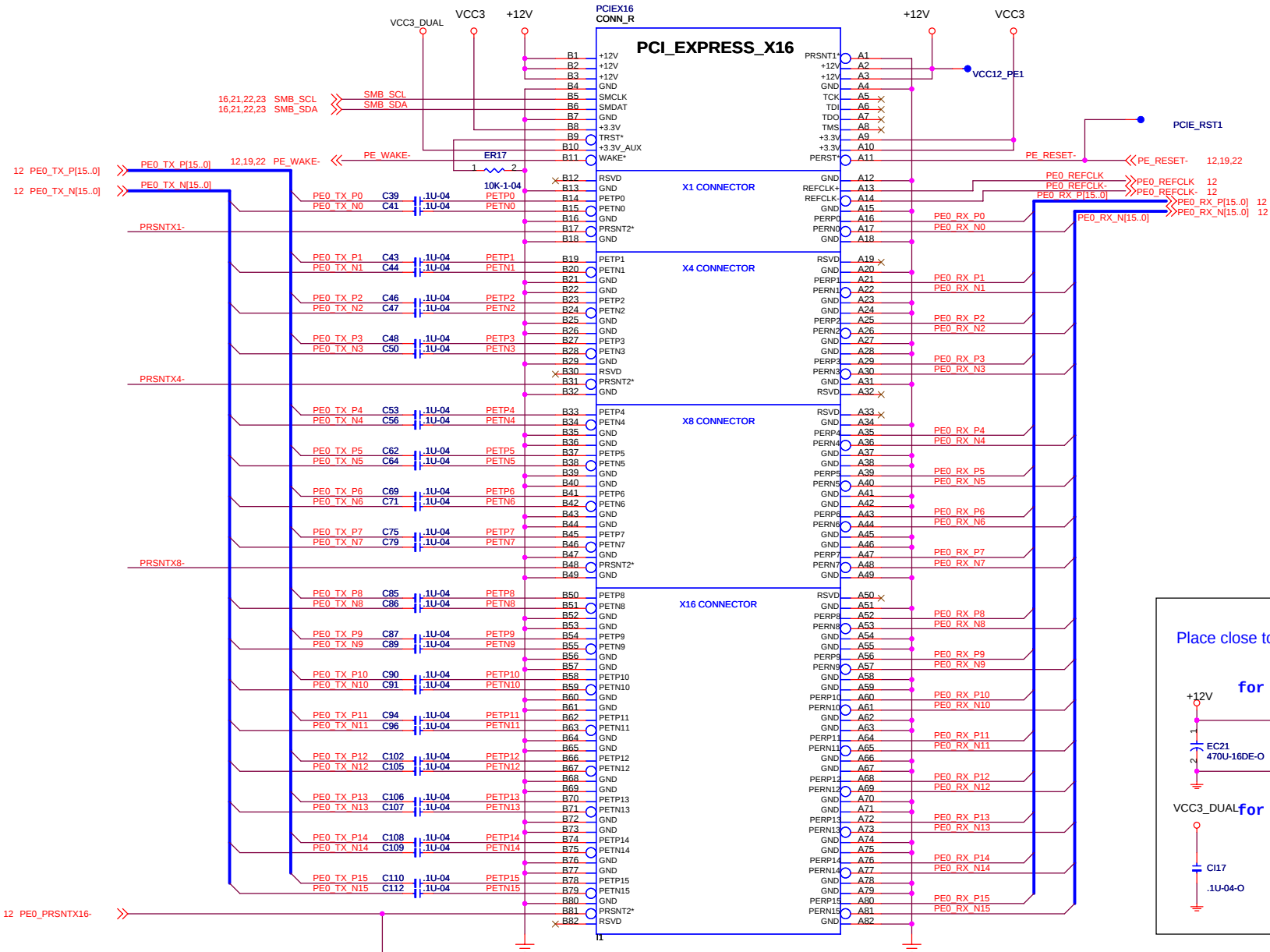
BOM Difference

	RTL8101E-GR 10/100M	RTL8111C-GR 1000M	RTL8111B-GR 1000M
Ca	RTL8101E-GR	RTL8111C-GR	RTL8111B-GR
Cb	V	X	X
Cc	X	V	X
Cd	2K-1-04	2.49K-1-04	2.49K-1-04
Ce	V	X	X
Cf	.01U-04	0-04	0-04
Cg	V	X	X
Ch	V	X	V
Ci	X	V	X
Cj	X	V	V
Ck	USBX2-LAN-100	USBX2-LAN-1000	USBX2-LAN-1000
Cm	X	X	HA8550-D
Cn1	X	X	HA8550-D
Cn2	0	5uH	X

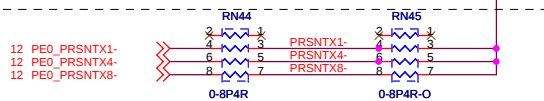
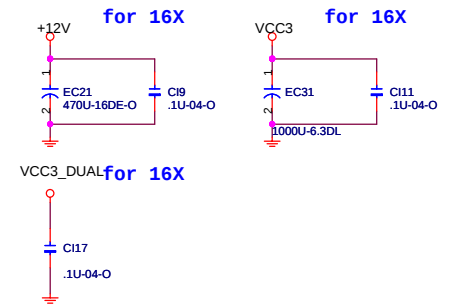
Power Difference

	RTL8101E/ RTL8111B	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V



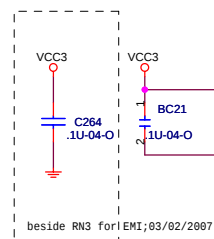
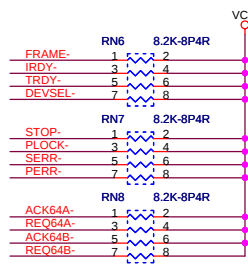
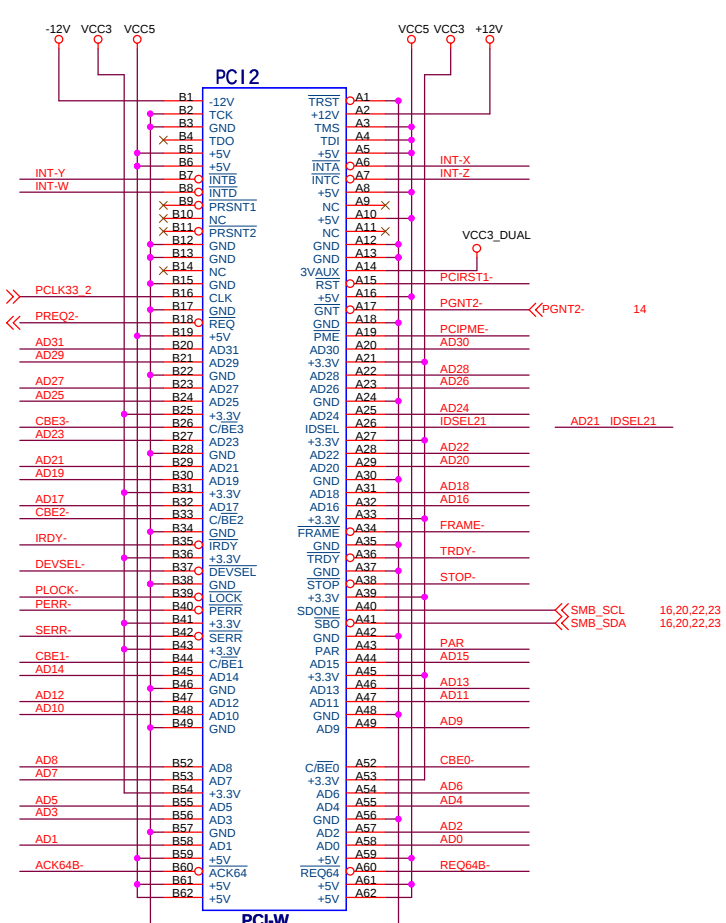
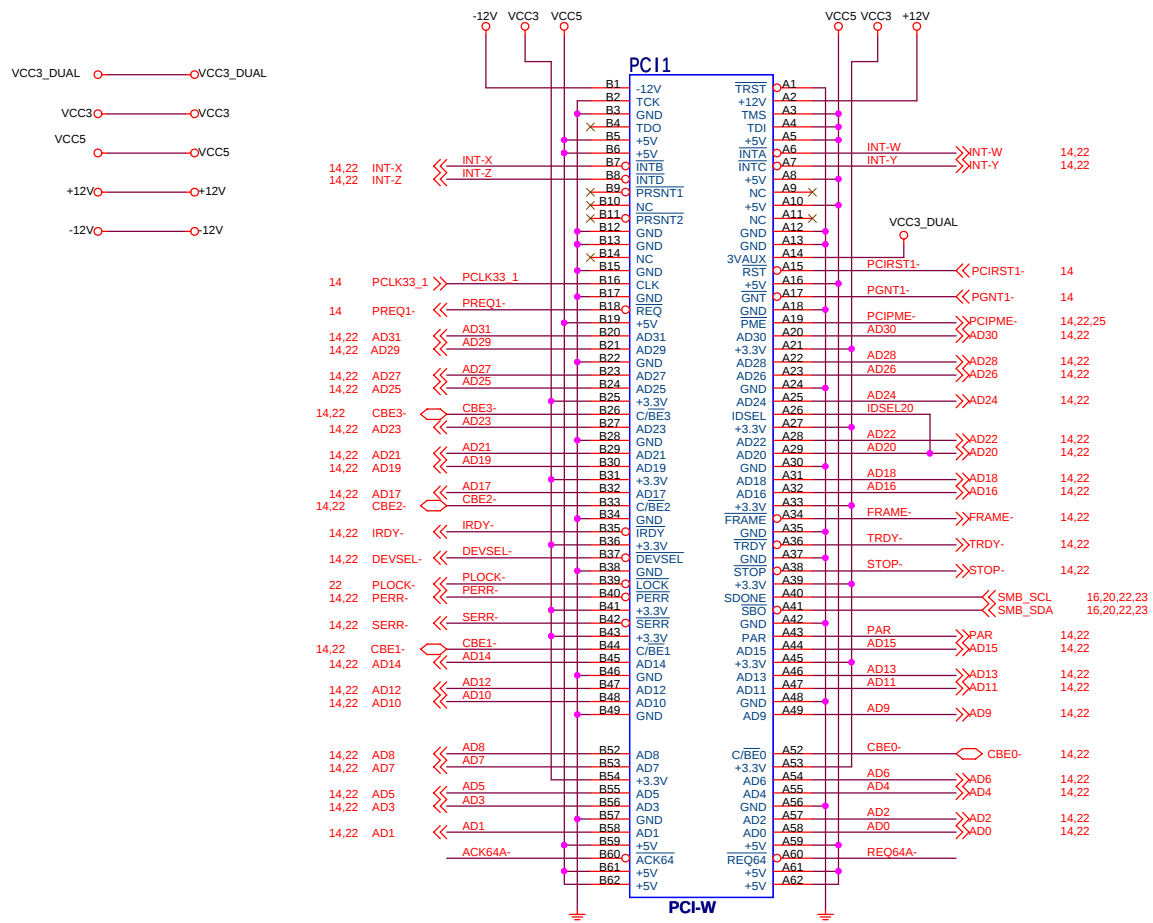


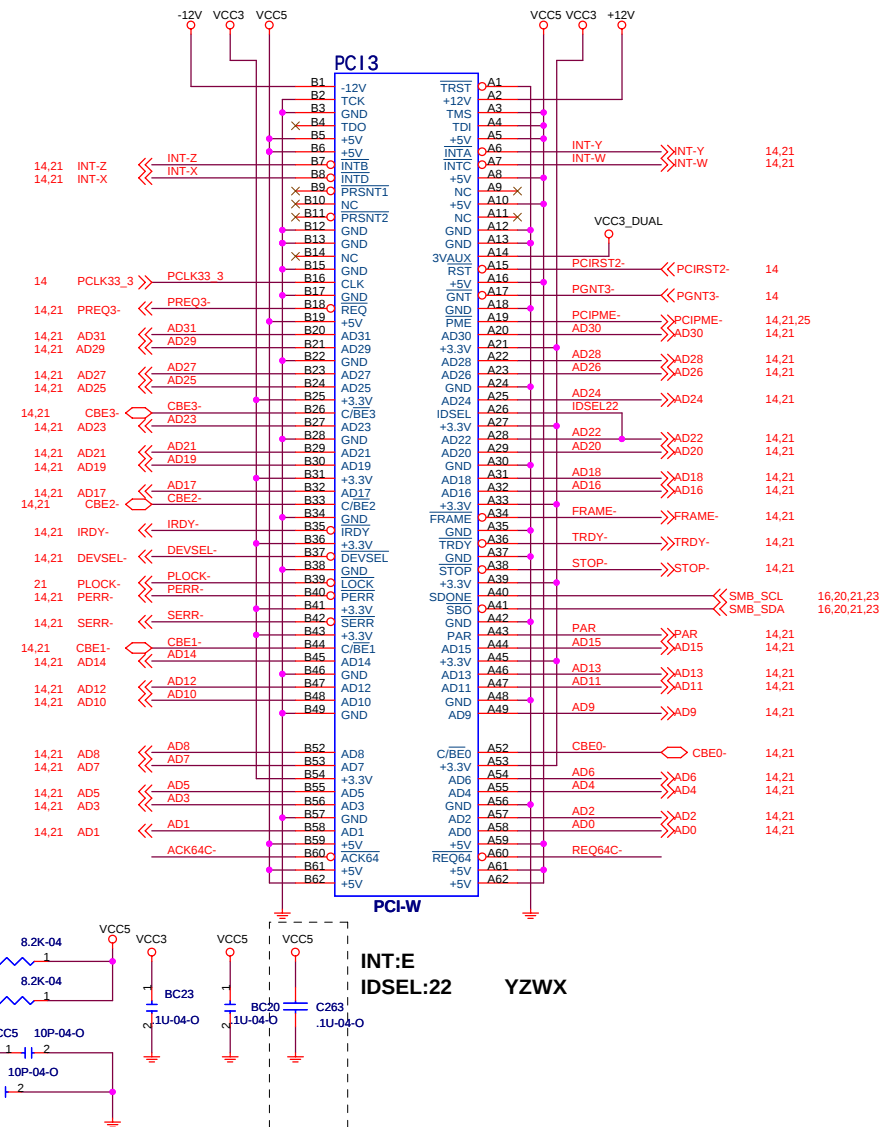
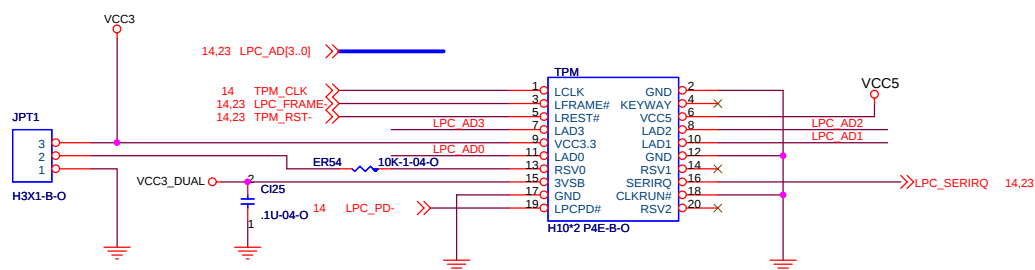
Place close to PCI EXPRESS connector as possible.

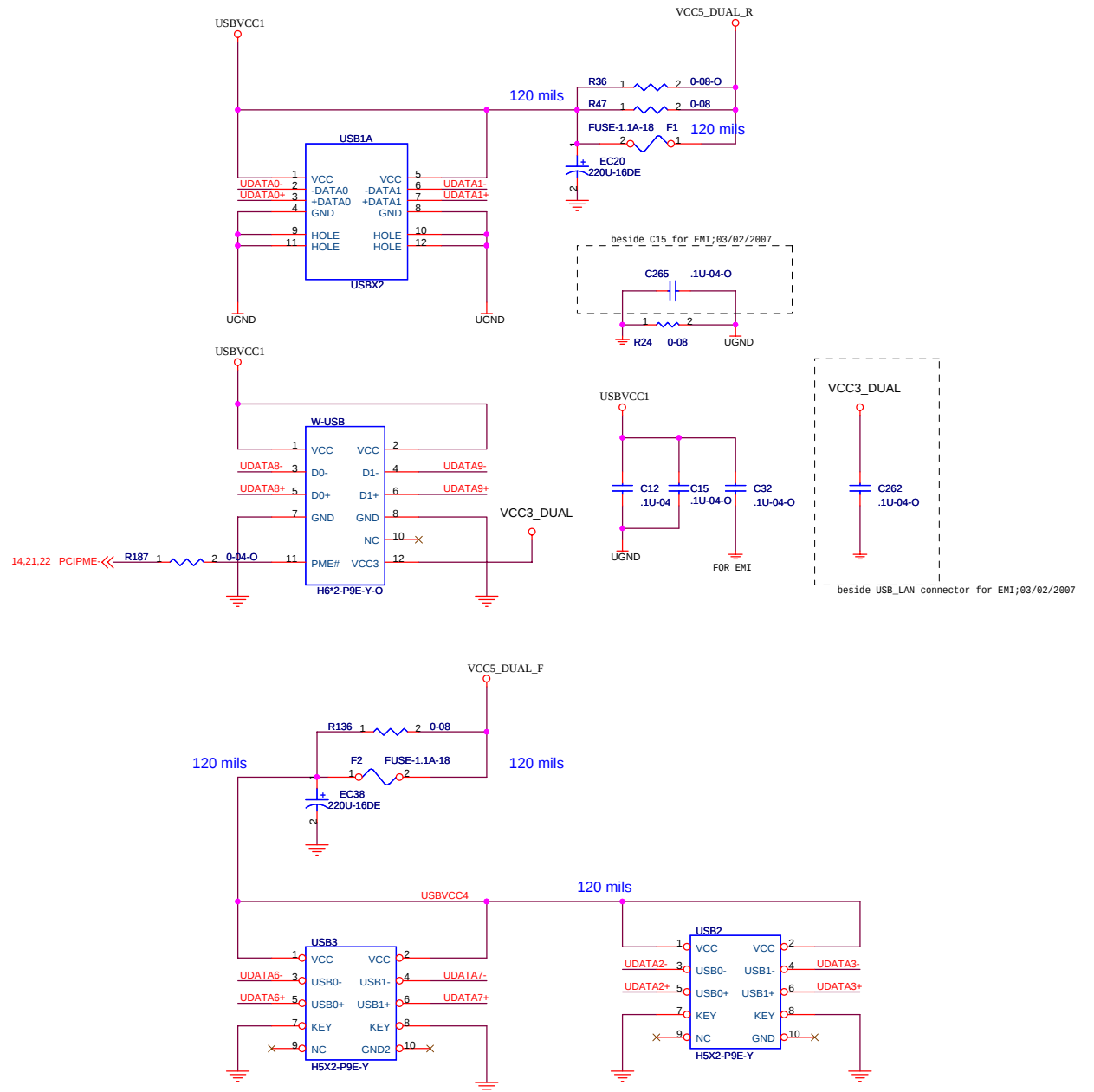
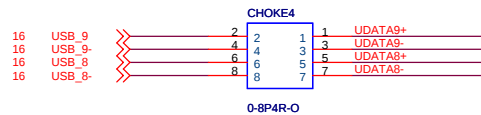
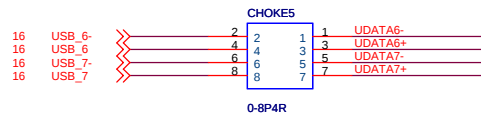
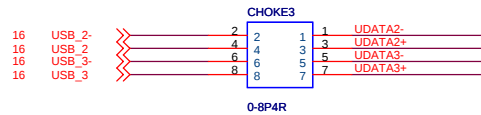
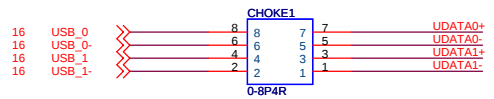


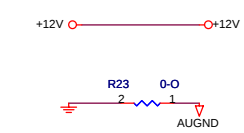
Fixed RN44 for MCP61D only; fixed RN44,RN45 for MCP65S ;02/27/2007

PCI-E X16 CONN		
Title Size Custom	Document Number NFORCE6M -A	Rev 2.0
Date: Tuesday, April 17, 2007		
Sheet 20 of 31		







[illegible]

Port	pin	signal	206	202
A	39,41	F-Line out	A	A
B	21,22	F-Mic in	B	B
C	23,24	R-Mic in	C	C
D	35,36	R-Line out	D	D
E	14,15	R-Surround	F	
F	16,17	R-Line in	E	F
G	43,44	R-Cen/Bass	G	
H	45,46	R-Side surr	H	
	18,20	CD In		
	48	SPDIF Out		

Location	92HD206	92HD207
Ca	X	820P-04
Cb	0-04	X
Cc	92H206	92HD202
Cd	V	X
Ce	AUDIO-6P	AUDIO-3P
Cg	X	V
Ch	V	X
Cl	V	X
CJ	V	X

The schematic diagram shows the output stage of the 74VHC04. It consists of two inverters. The first inverter's input is connected to VCCR. Its output is connected to PORT-C R. The second inverter's input is also connected to VCCR. Its output is connected to PORT-C L. Both inverters have their inputs connected to a pull-up network consisting of a 4.7K-04 resistor and a 1U-06 capacitor in parallel. The outputs are connected to AUGND.

Place near Chip

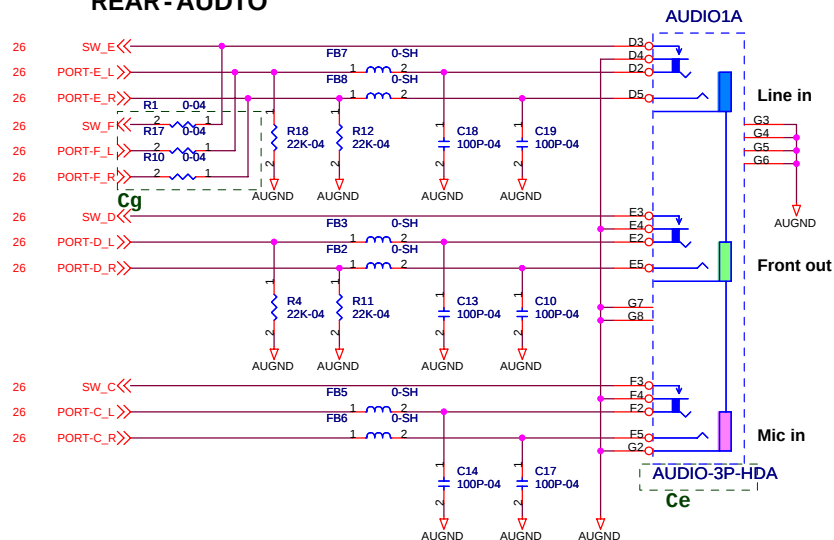
The schematic diagram shows the Sense Amplifier circuit. It includes a +5V_A supply, a SENSEA input, and three resistors: ER11 (5.1K-1-04), ER10 (5.1K-1-04), and ER9 (10K-1-04). A capacitor C16 (2000P-04) is connected to the output of the resistors. The circuit is connected to a common ground labeled AUGND. The outputs are SW_D, SW_C, and FSENSE.

The diagram shows the SenseB input circuit. It consists of a 5V supply connected to a series of resistors: ER5 (5.1K-1.04), ER4 (5.1K-1.04-0), ER3 (10K-1.04-0), ER2 (20K-1.04), and ER1 (39.2K-1.04-0). A capacitor C2 (2000P-04) is connected to ground. The output is labeled SENSEB. The diagram is annotated with 'Cj' and '27'.

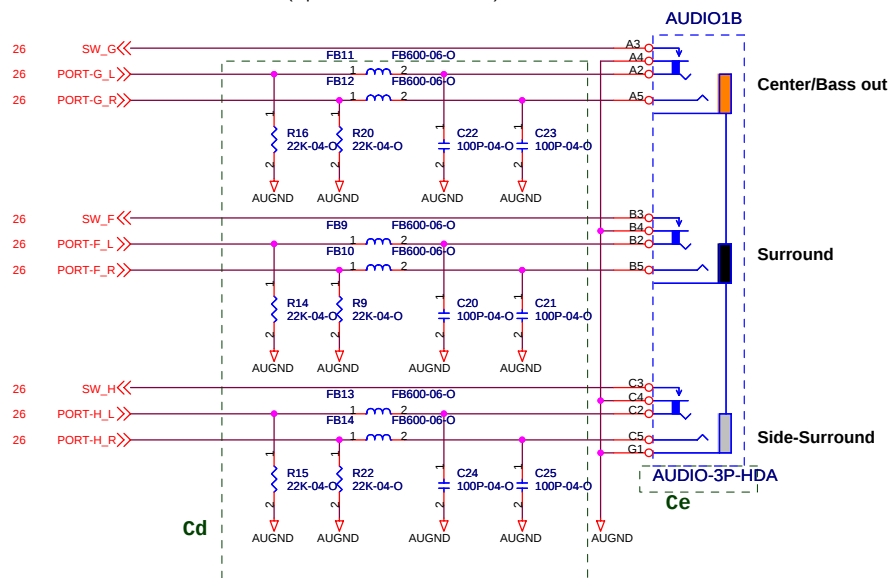
External Connection

VCC5

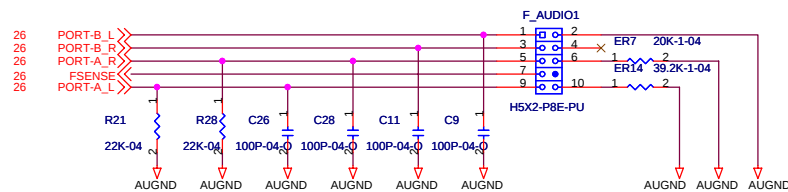
REAR-AUDIO



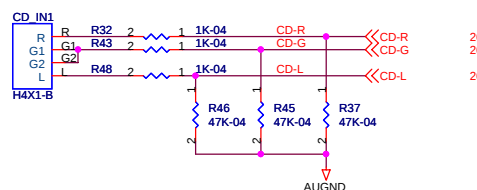
(Optional Rear Audio Panel)



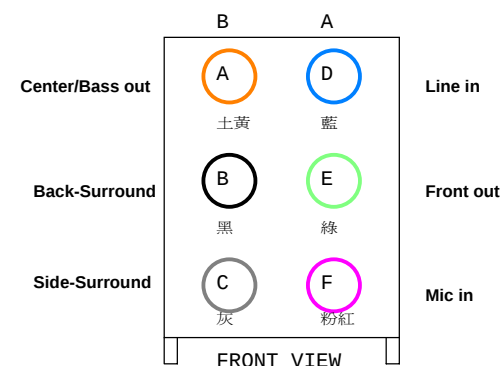
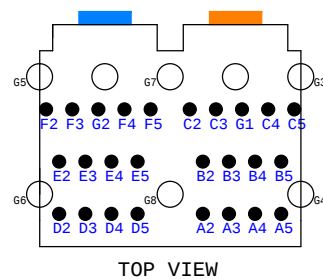
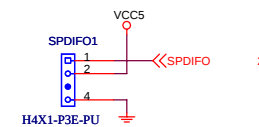
FRONT-AUDIO

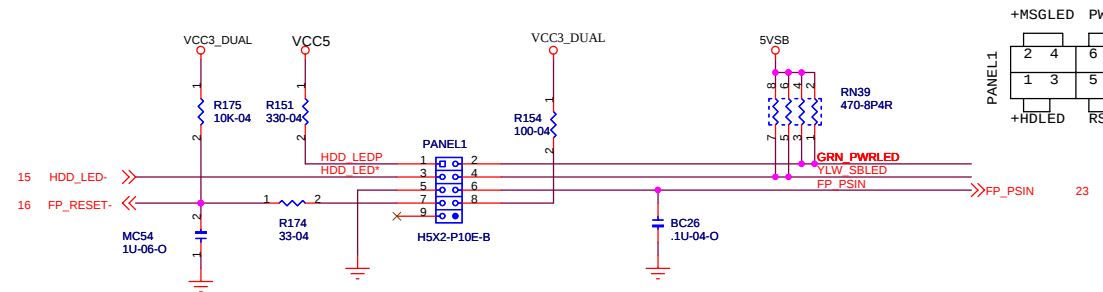
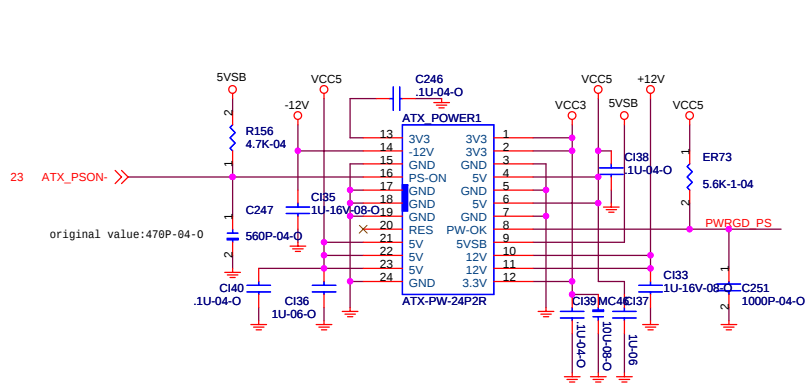


CD_IN

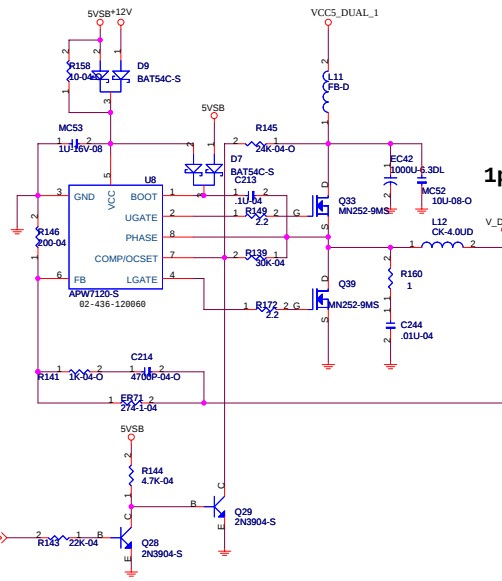


SPDIF-OUT



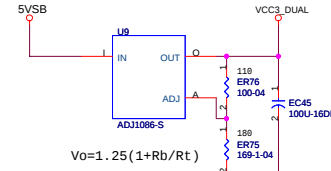


R345	RT92B2	RT9214
U30	X	V
R344	X	30K
R752	25K	X



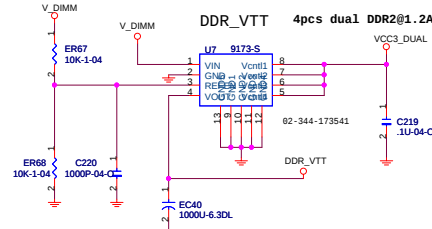
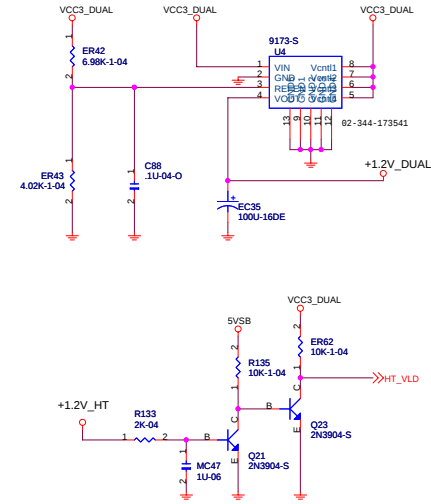
1pcs DDR2@2.5A

+3.3V_DUAL

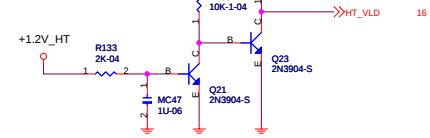


$$V_0 = 1.25(1 + R_b/R_t)$$

MCP61 AUX(1.2V) @250mA



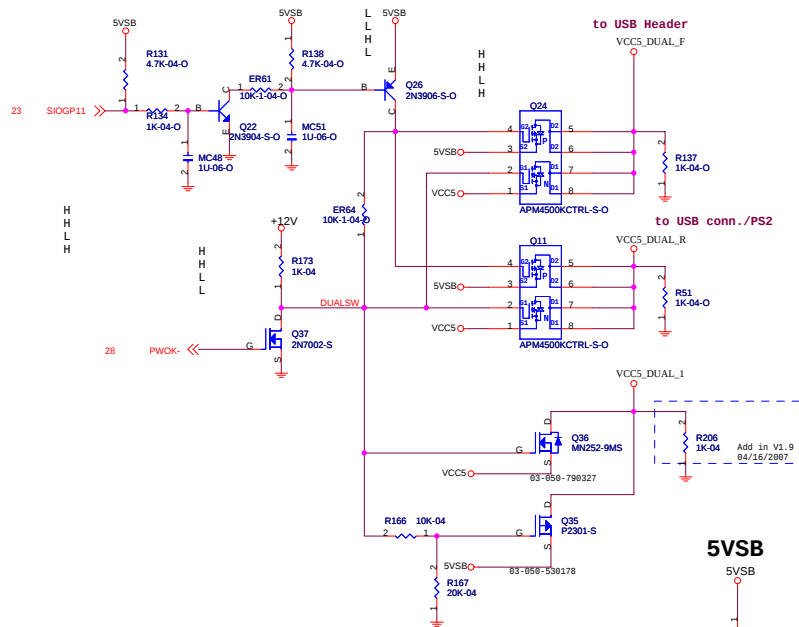
DDR_VTT 4pcs dual DDR2@1.2A



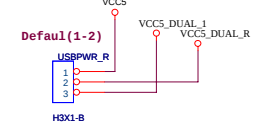
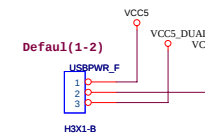
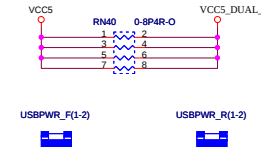
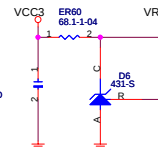
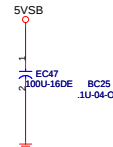
KEYBOARD/MOUSE POWER ON

SI0GP11	S0	S1	S3	S4/S5
USE	H	H	L	L
UN-USE	H	H	L	H

+5V_DUAL FOR USB, PS2



5VSB



USBPWR_F / R
1-2 VCC5
2-3 VCC5_DUAL

5

4

3

2

1

PCI_SLOT1 : REQ0, GNT0, CLK0, AD21, INT WXYX

PCI_SLOT2 : REQ1, GNT1, CLK1, AD22, INT XYZW

PCI_1394 : REQ2, GNT2, CLK2, AD25, INT Z

PCI_LAN : REQ3, GNT3, CLK3, AD24, INT Y

04/17/2007 V2.0

I/O GP_RESERVE1 is used to detect the M/B' s Version.

GP_RESERVE1 = 1, Version = 1.0

GP_RESERVE1 = 0, Version = 2.0

LOCATION	REMARK	MCP65S	MCP61D
NV1		01-201-065950	01-201-061980
R176	TP_MCP61_TRST	X	05-152-100103
RN45	FOR PCI-E 16X	06-841-000080	X
CHOKE4	FOR W-USB	06-841-000080	X
R187	FOR W-USB	05-152-000100	X
W-USB	FOR W-USB	10-342-012387	X
SATA3	FOR SATA	10-020-007697	X
C5, C6, C7, C8 . , C242, C250, C255, C261	FOR SATA	04-884-103203	X
ESATA	FOR SATA	10-090-007011	X
R152, R155, R161, R162	FOR SATA	05-152-000100	X

PCI-E LAN BOM

LOCATION	RTL8101E-R	RTL8111C-GR	RTL8111B-GR
LAN1	01-267-101350		01-267-111350
FB21	05-112-000000	X	X
FB19	X	16-101-121373	X
ER77	05-152-200112	05-152-249112	05-152-249112
R193, R194	05-152-000100	X	X
C269	04-884-103203	05-152-000100	05-152-000100
ER78, ER79, ER80, ER81	05-152-499110	X	X
C281, C289	04-887-104105	X	X
R199	05-112-000000	X	05-112-000000
R201, R203, R204	05-152-000100	X	05-152-000100
R198, R200	X	05-112-000000	X
R202, R205	X	05-152-000100	X
R195	X	05-152-470102	05-152-470102
Q40	X	03-070-590426	03-070-590426
USBLAN1	10-084-022522	10-084-022503	10-084-022503
Q41, Q42	X	X	03-070-355052
FB20	05-112-000000	05-112-000000	X



Elitegroup Computer Systems

Title

ATTENTION

Size

Document Number

Rev

Custom

NFORCE6M -A

2.0

Date:

Wednesday, April 18, 2007

Sheet

31

of

31