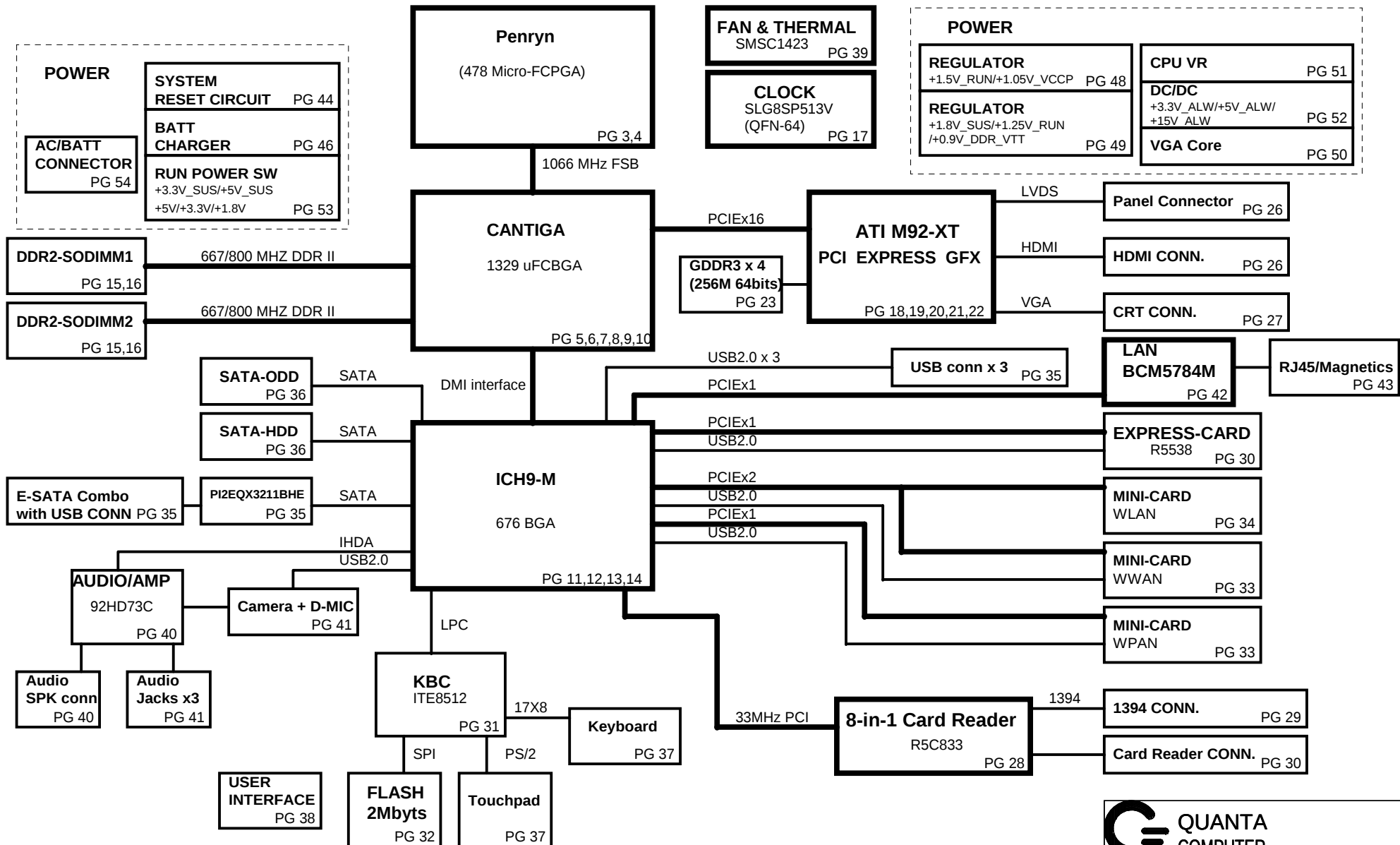


FM8 Hanks Intel Discrete GFX

VER : 3A

PWA:W021J

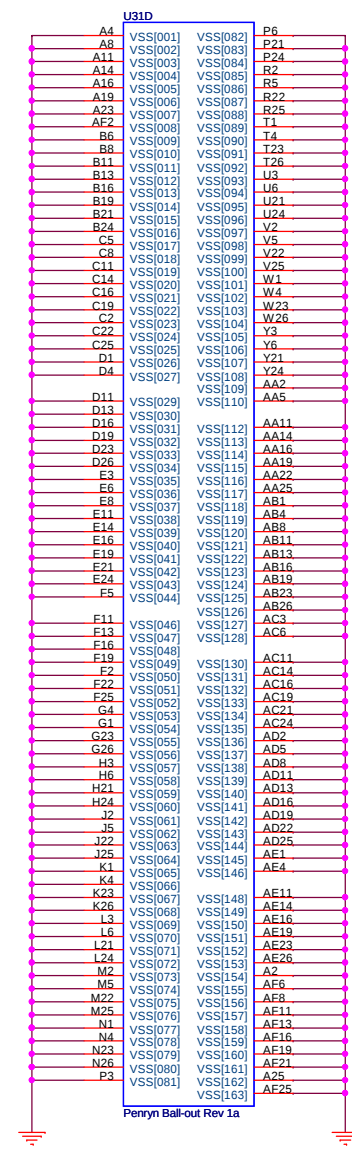
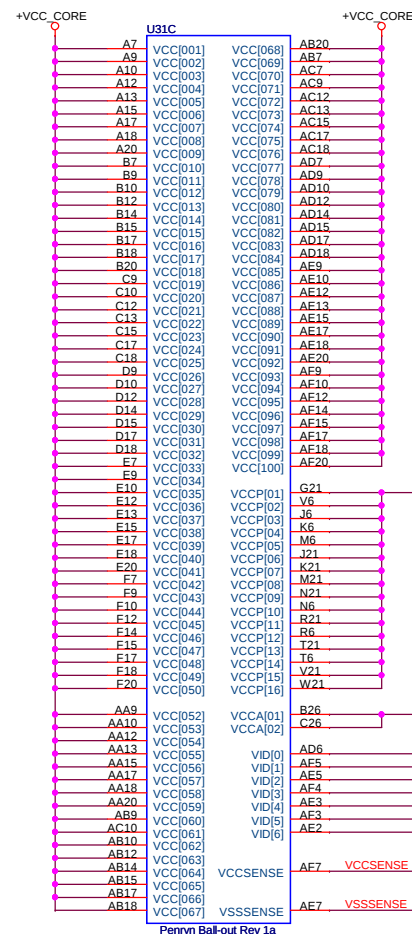
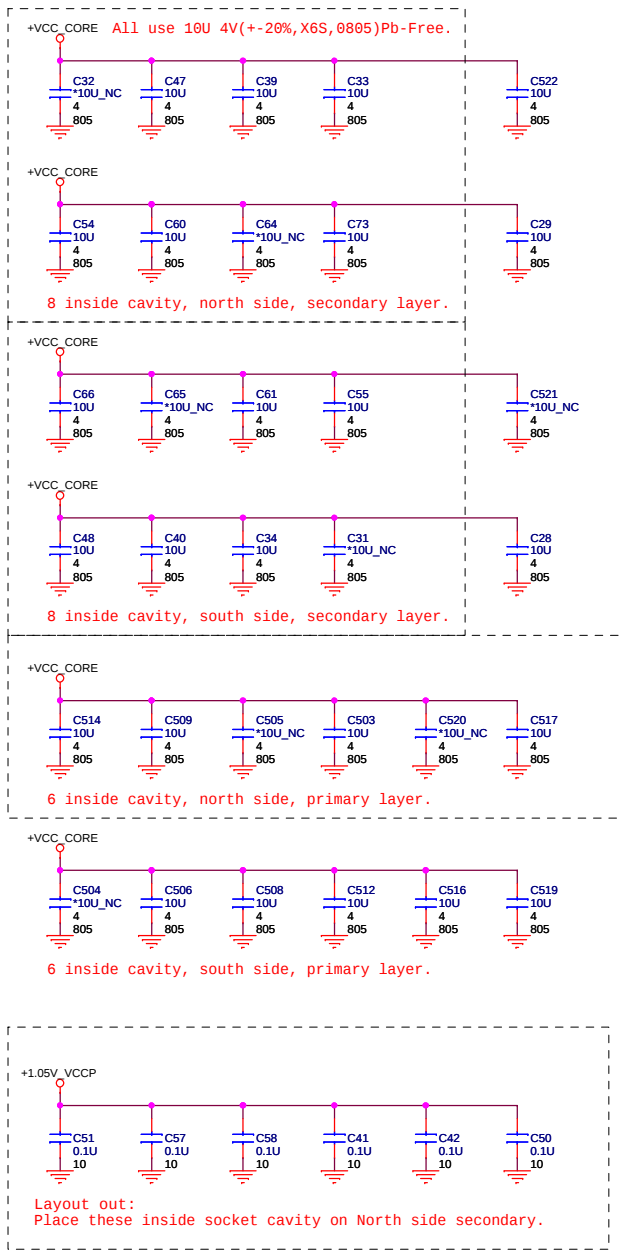
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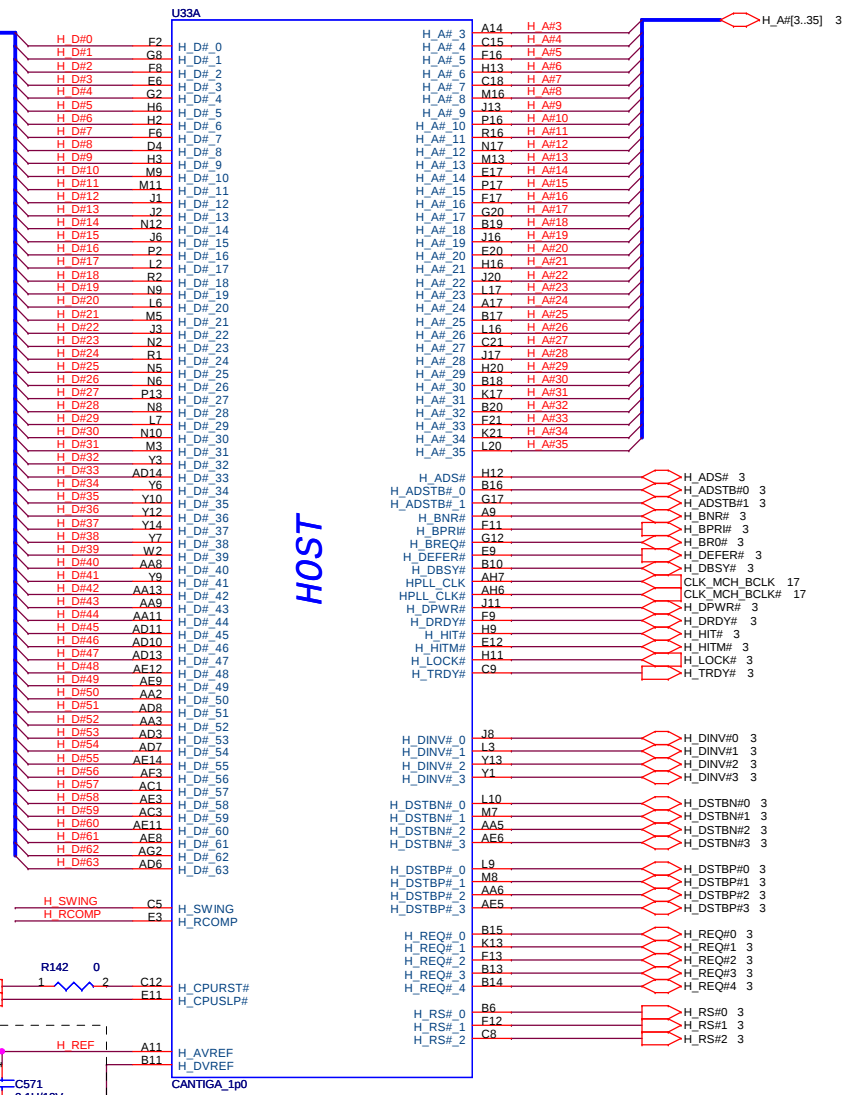
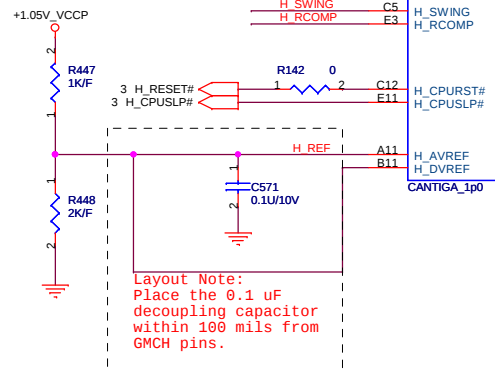
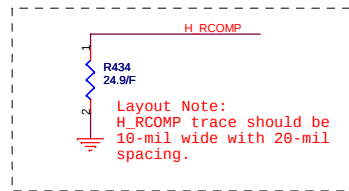
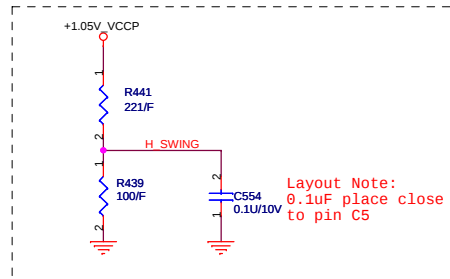


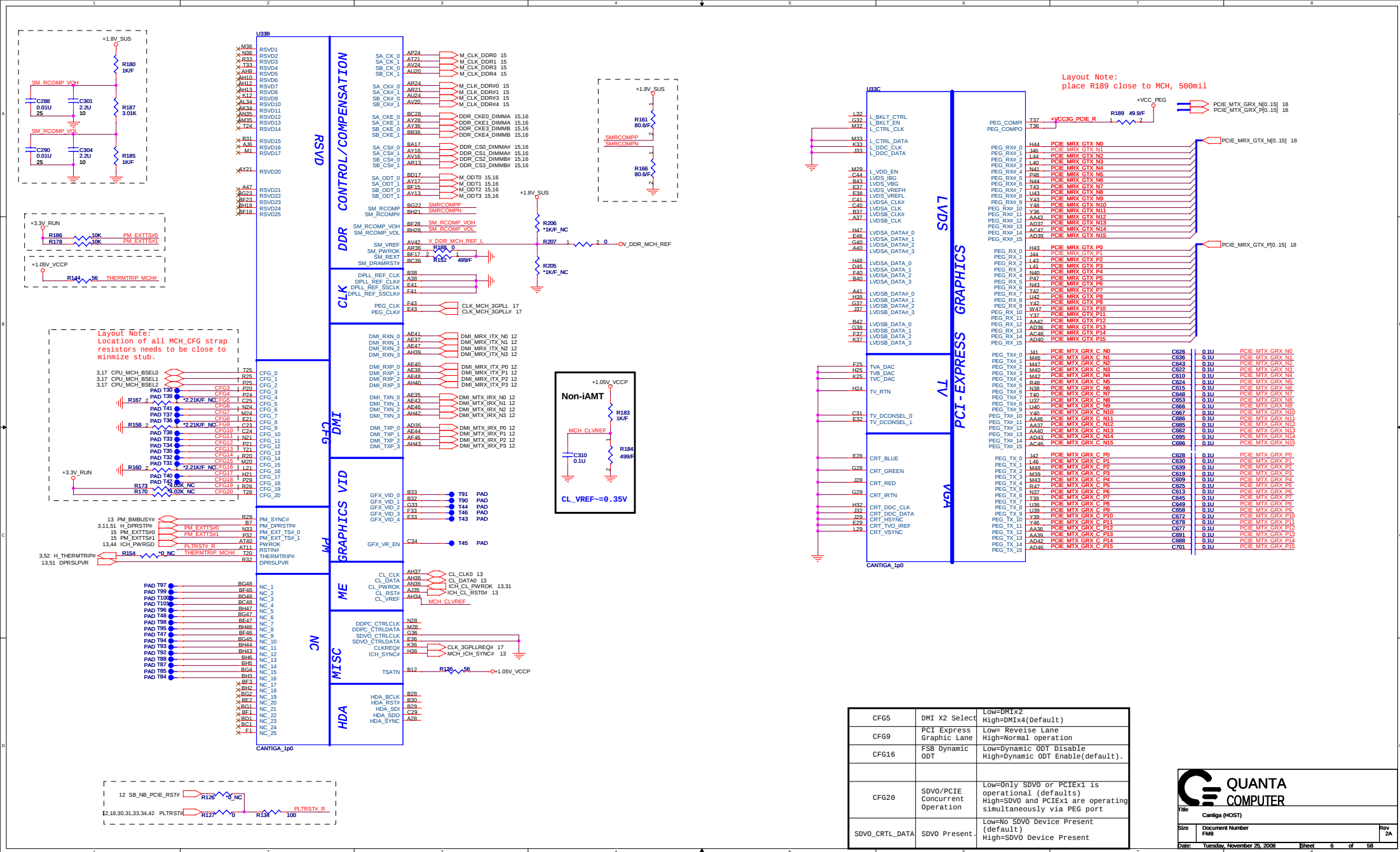
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-4	Penryn
5-10	Cantiga
11-14	ICH9M
15-16	DDRII SO-DIMM(200P)
17	Clock Generator
18-23	M92-S2-XT
24	BLANK PAGE
25	BLANK PAGE
26	LCD CONN / HDMI CONN
27	CRT CONN
28	5C833/PCI
29	IEEE1394
30	Express/Card Reader
31	SIO (ITE8512)
32	FLASH / RTC
33	MINI-Card (WPAN, WWAN)
34	MINI-Card (WLAN)
35	USB
36	SATA (HDD & CD_ROM)
37	TP / KEYBOARD
38	SWITCH / LED
39	FAN / THERMAL
40	Azelia CODEC
41	AUDIO CONN
42	LAN (RTL8111B/8111C)
43	LAN RJ-45 / TRANSFORM
44	System Reset Circuit
45	Blank Page
46	Changer (MAX8731A)
47	Blank Page
48	1.05VCCP & 1.5VRUN
49	1.8VSUS & 0.9VTT
50	VGA_M82
51	CPU_ISL6266 (2PHASE)
52	MAX8744 (+5V,3.3V)
53	Run Power Switch
54	DCin & Batt
55	PAD & SCREW
56	EMI CAP
57	SMBUS BLOCK
58	Power Block Diagram

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,46,48,49,50,51,52	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,31,32,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW2	+5V	38,48,49,52,53,54	LARGE POWER	RUN_ON	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,35,36,38,50,51,52,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,26,30,38,43,48,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53	SODIMM POWER	SUS_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	14,20,26,27,36,37,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,6,8,9,11,12,13,14,15,17,20,22,26,27,28,30,31,33,34,36,39,40,41,42,51,53	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,31,33,34,48,53	CALISTOGA/ICH9 POWER	RUN_ON	
+1.2V_LOM	+1.25V	42	LOM POWER	+3.3V_LAN	
+1.1V_GFX_PCIE	+1.1V	21,50	VGA POWER	RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN	
+5V_HDD	+5V	36	HDD Power	HDDC_EN	

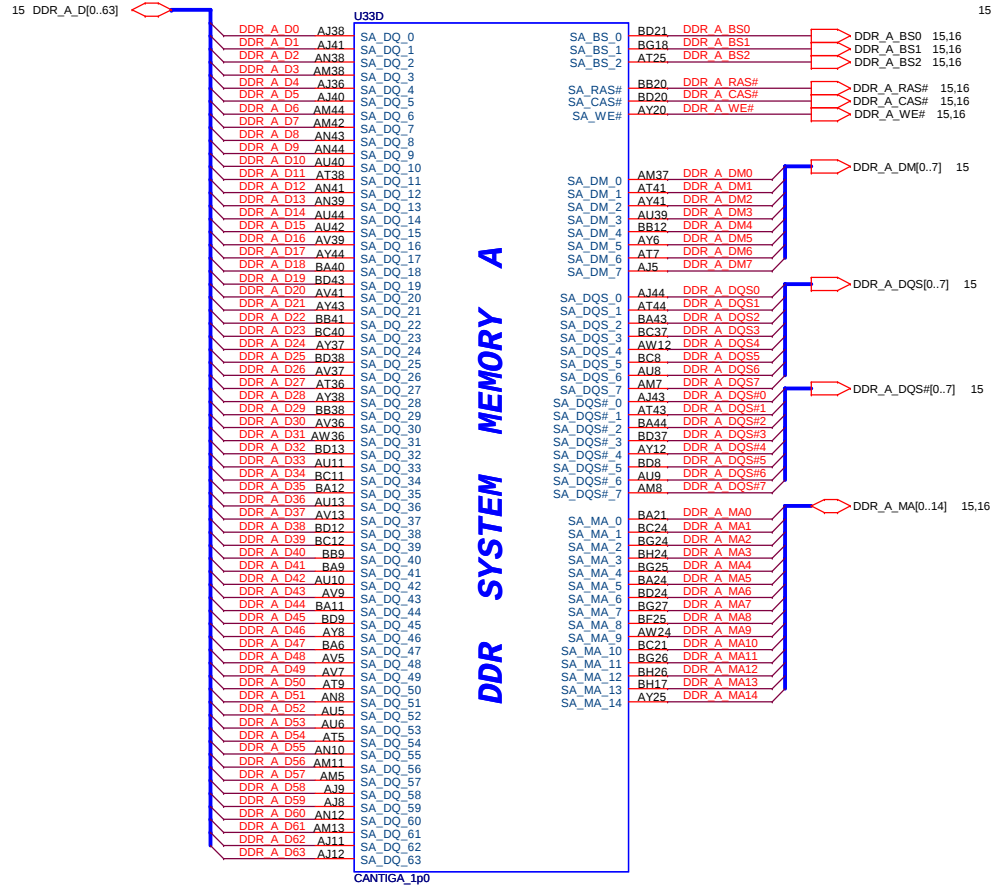
GND PLANE	PAGE	DESCRIPTION
 GND_CHG	46	
 GND_1.05V	47	
 GND_VGA	50	
 GND_SIGNAL	51	
 AGND_DC/DC	52	
 GND	ALL	



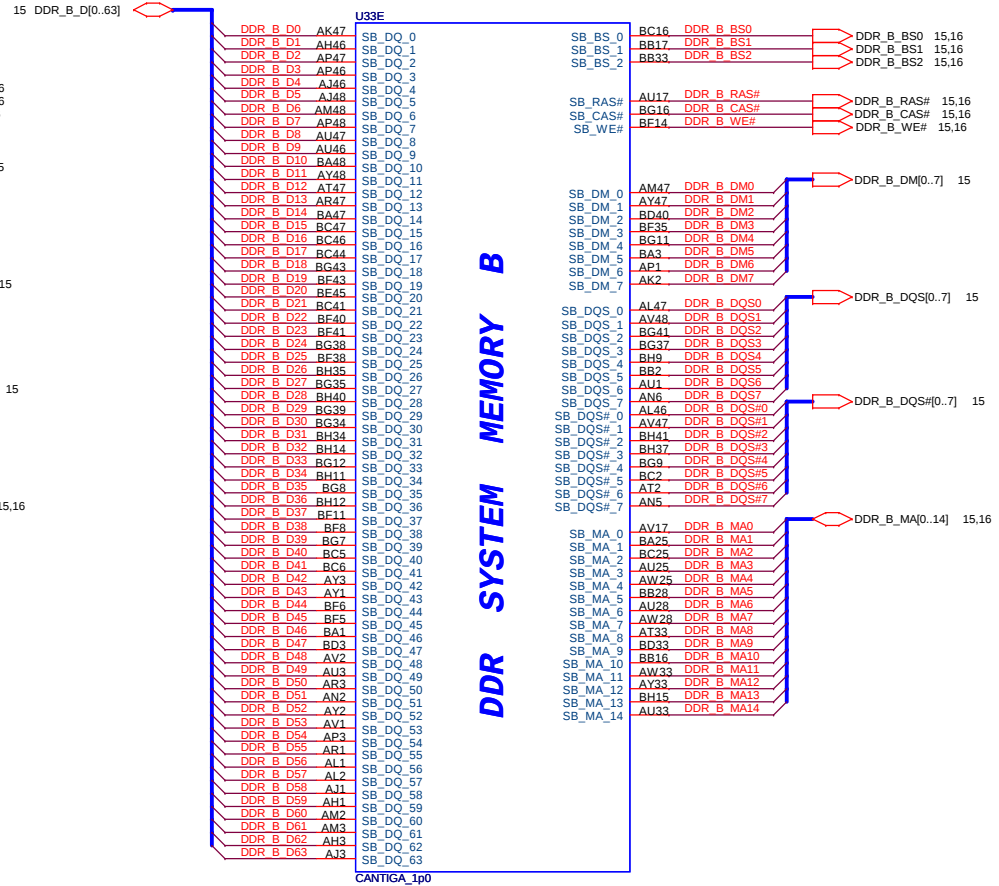




CFG5	DMI X2 Select	Low=DMIX2 High=DMIX4(Default)
CFG9	PCI Express Graphic Lane	Low= Reverse Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG20	SDVO/PCIe Concurrent Operation	Low=Only SDVO or PCIe1 is operational (defaults) High=SDVO and PCIe1 are operating simultaneously via PEG port
SDVO_CTRL_DATA	SDVO Present.	Low=No SDVO Device Present (default) High=SDVO Device Present

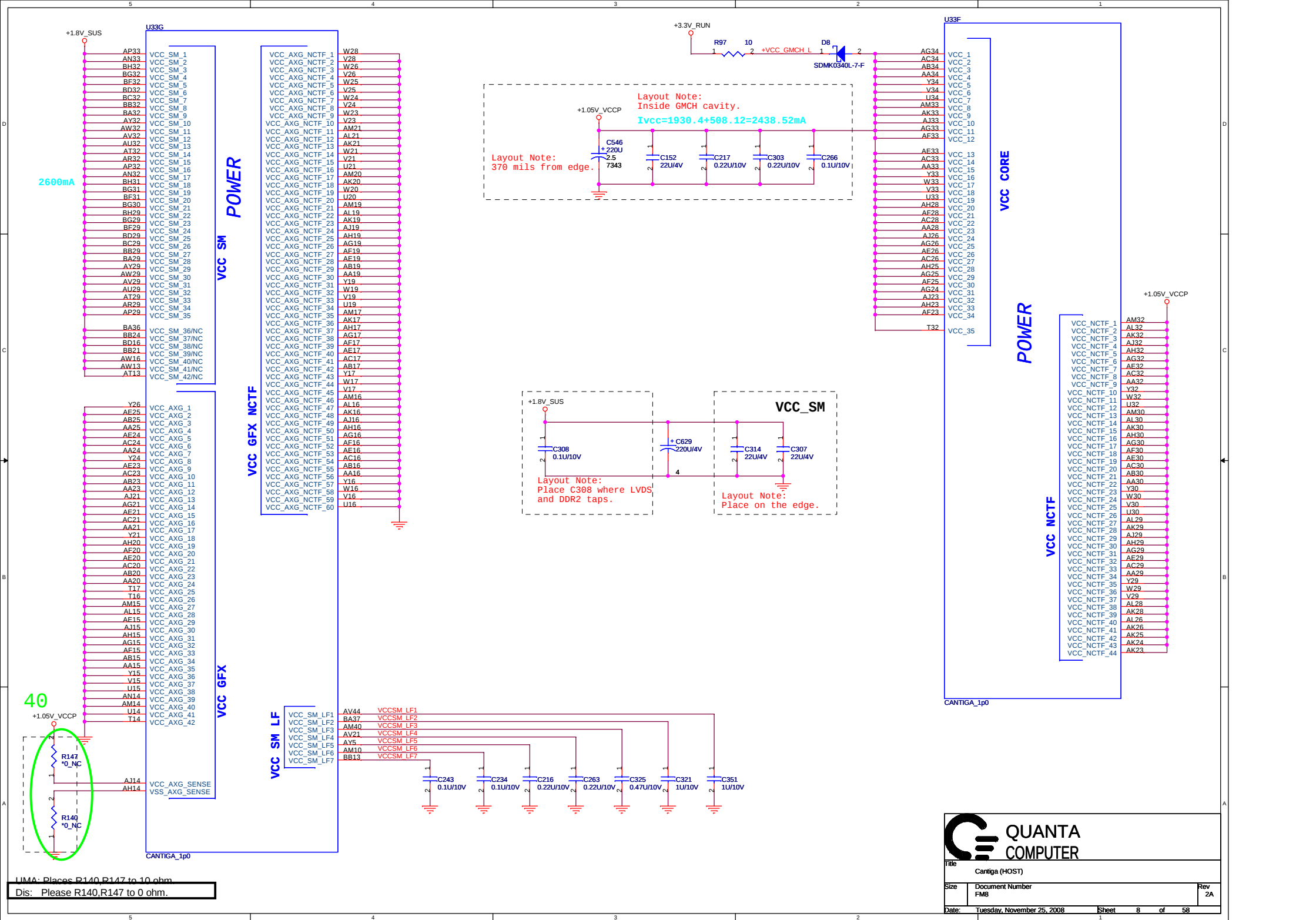


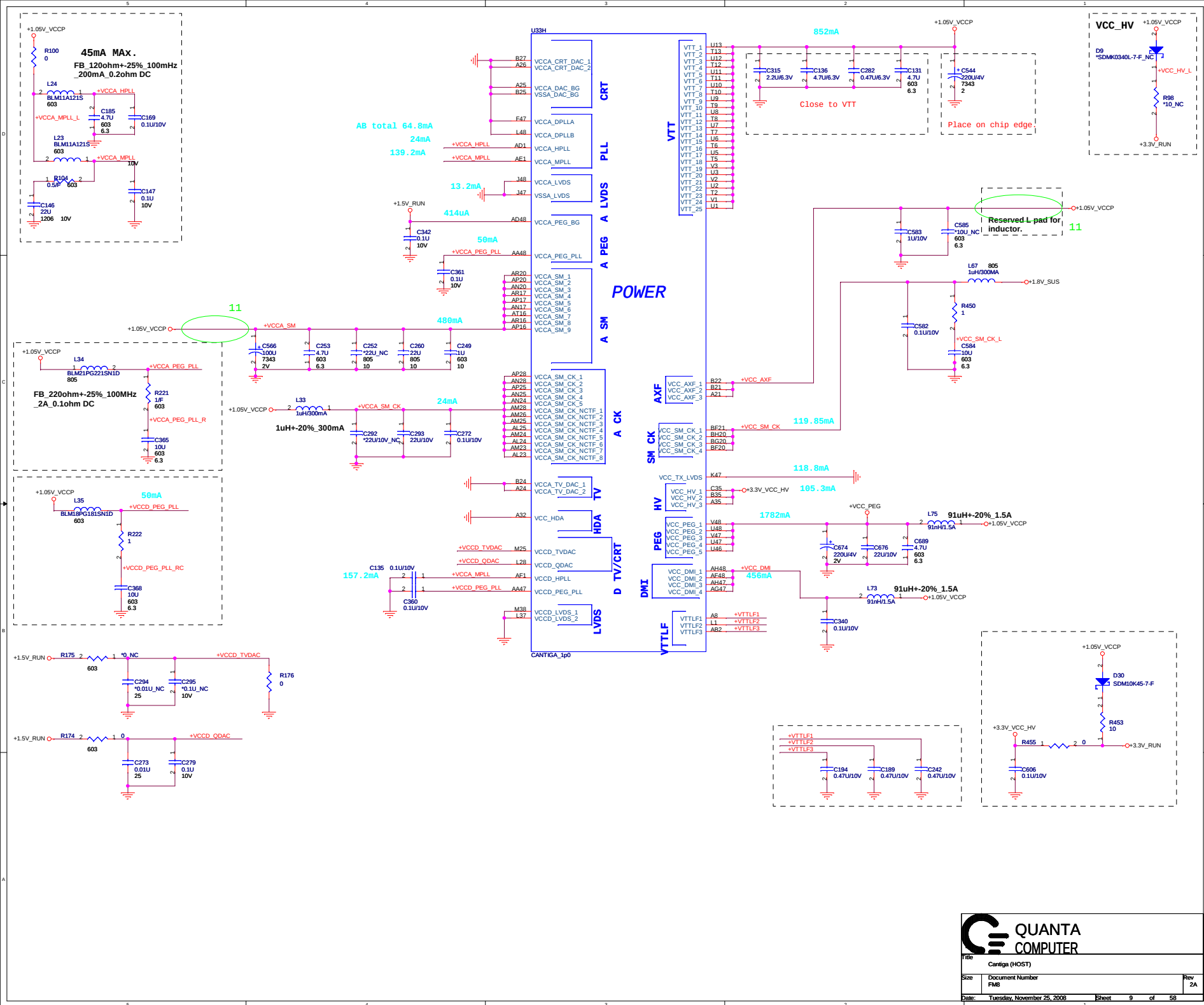
DDR SYSTEM MEMORY A

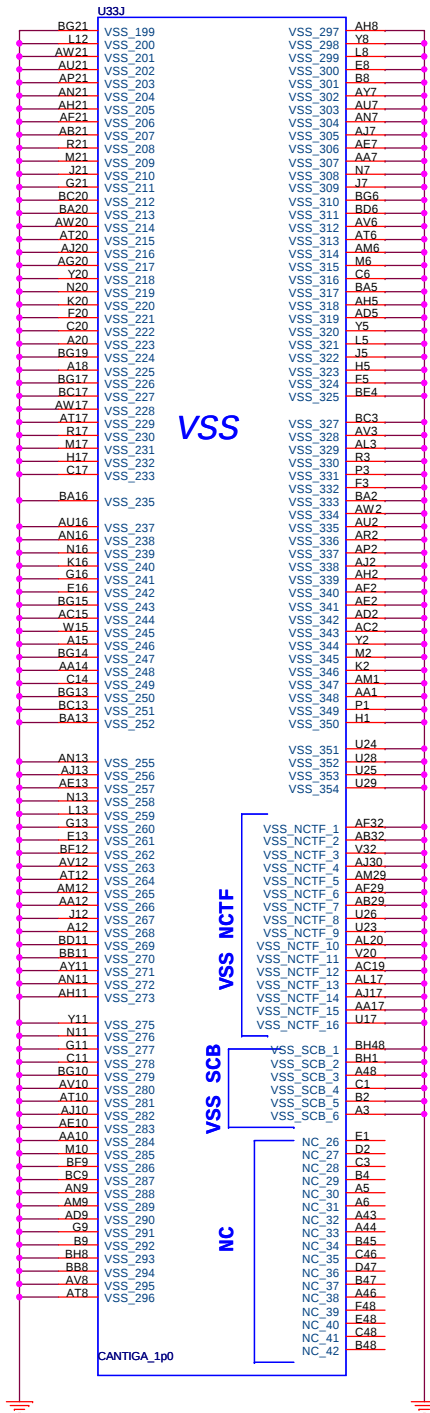
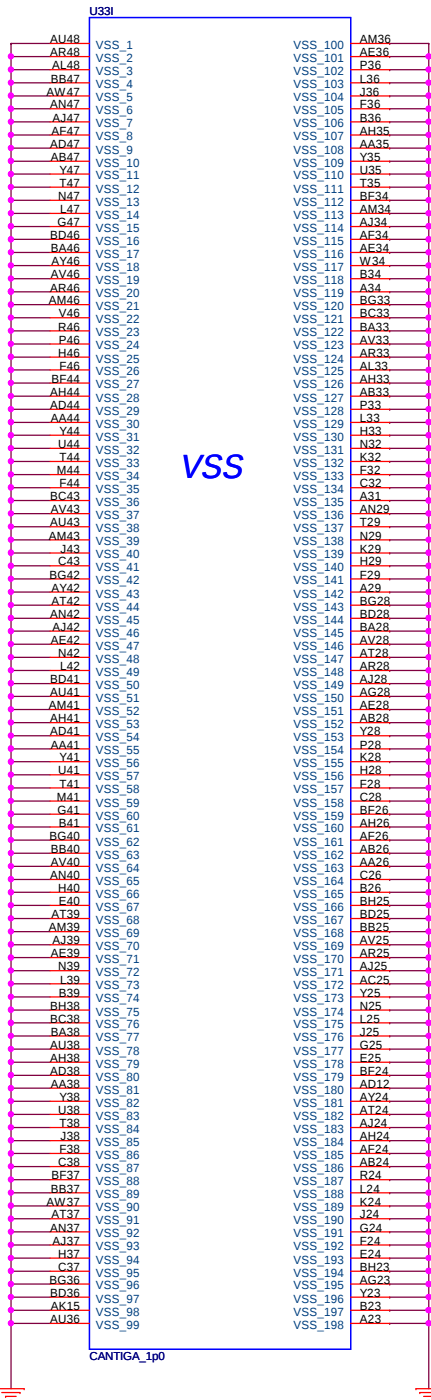


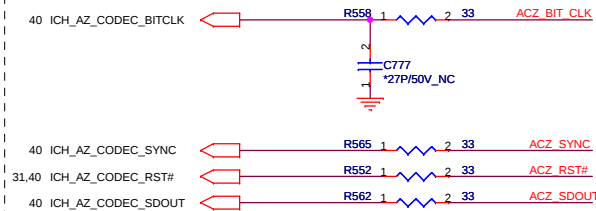
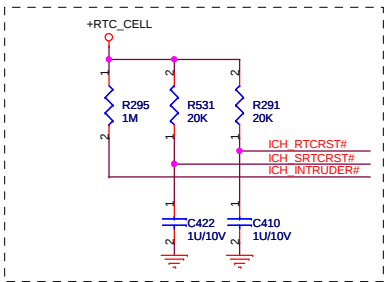
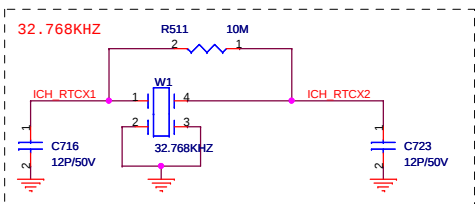
DDR SYSTEM MEMORY B



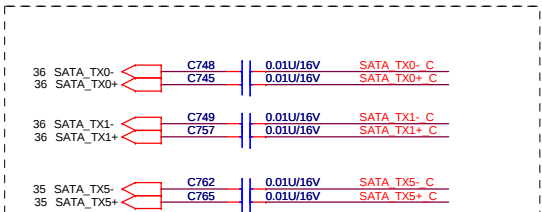




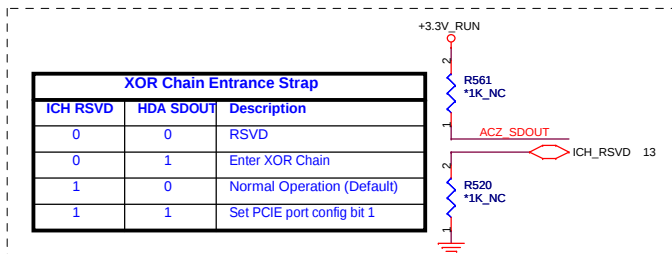
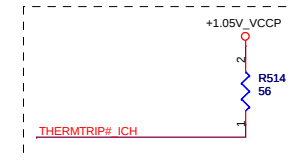
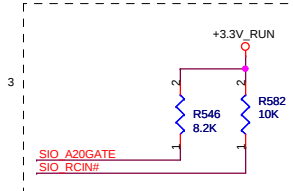
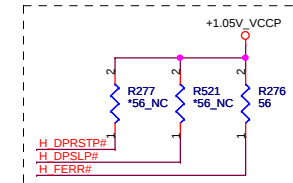
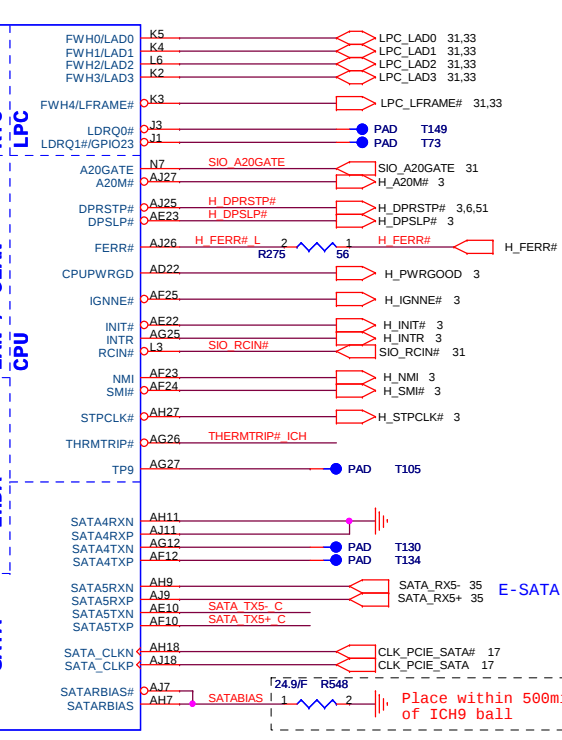
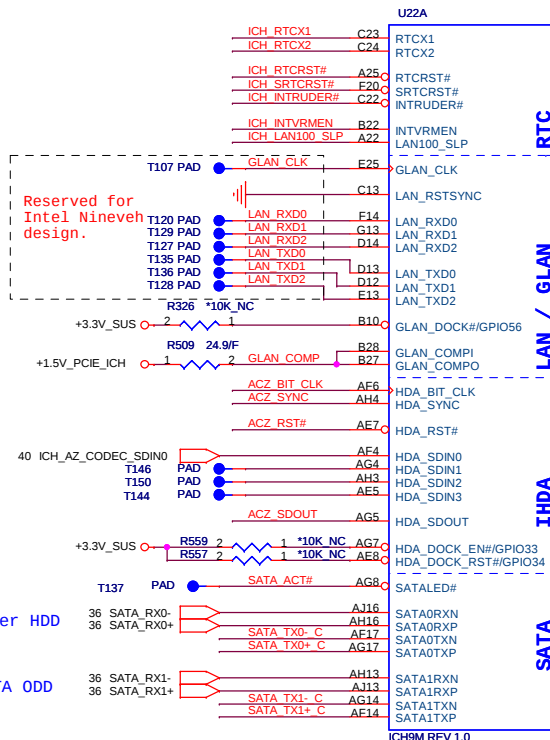
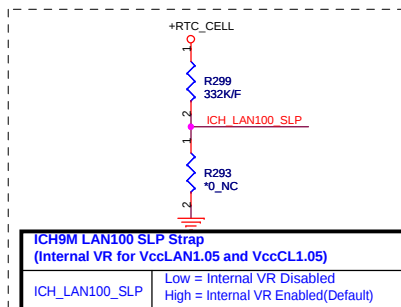
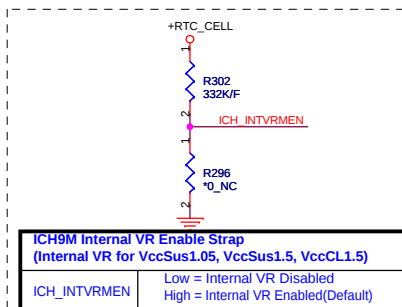




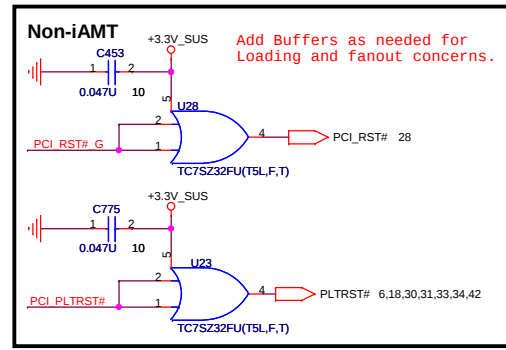
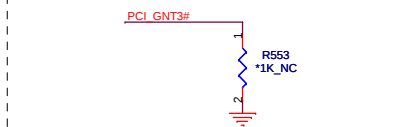
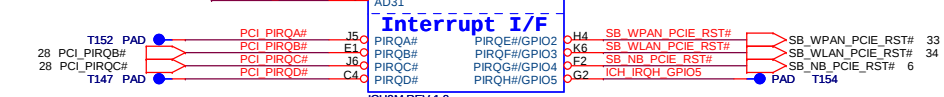
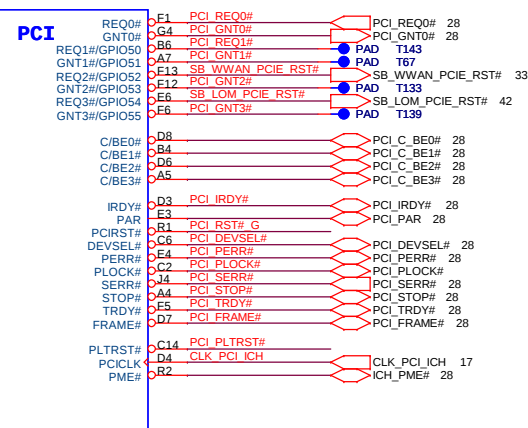
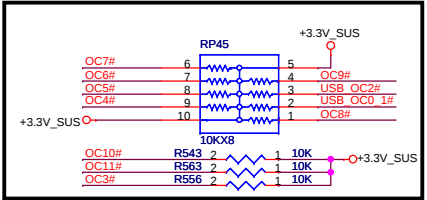
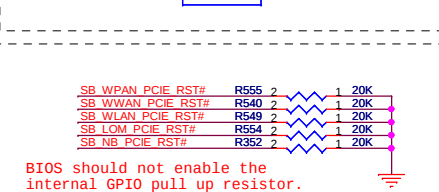
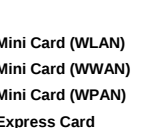
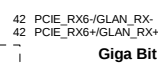
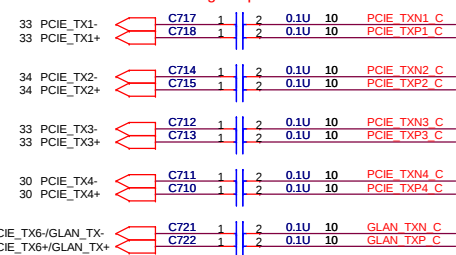
Place all series terms close to ICH9 except for SDIN input lines, which should be close to source. Placement of R558, R565, R552 & R562 should equal distance to the T split trace. Basically, keep the same distance from T for all series termination resistors.



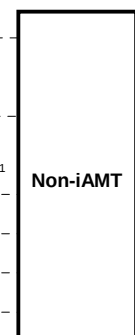
Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.

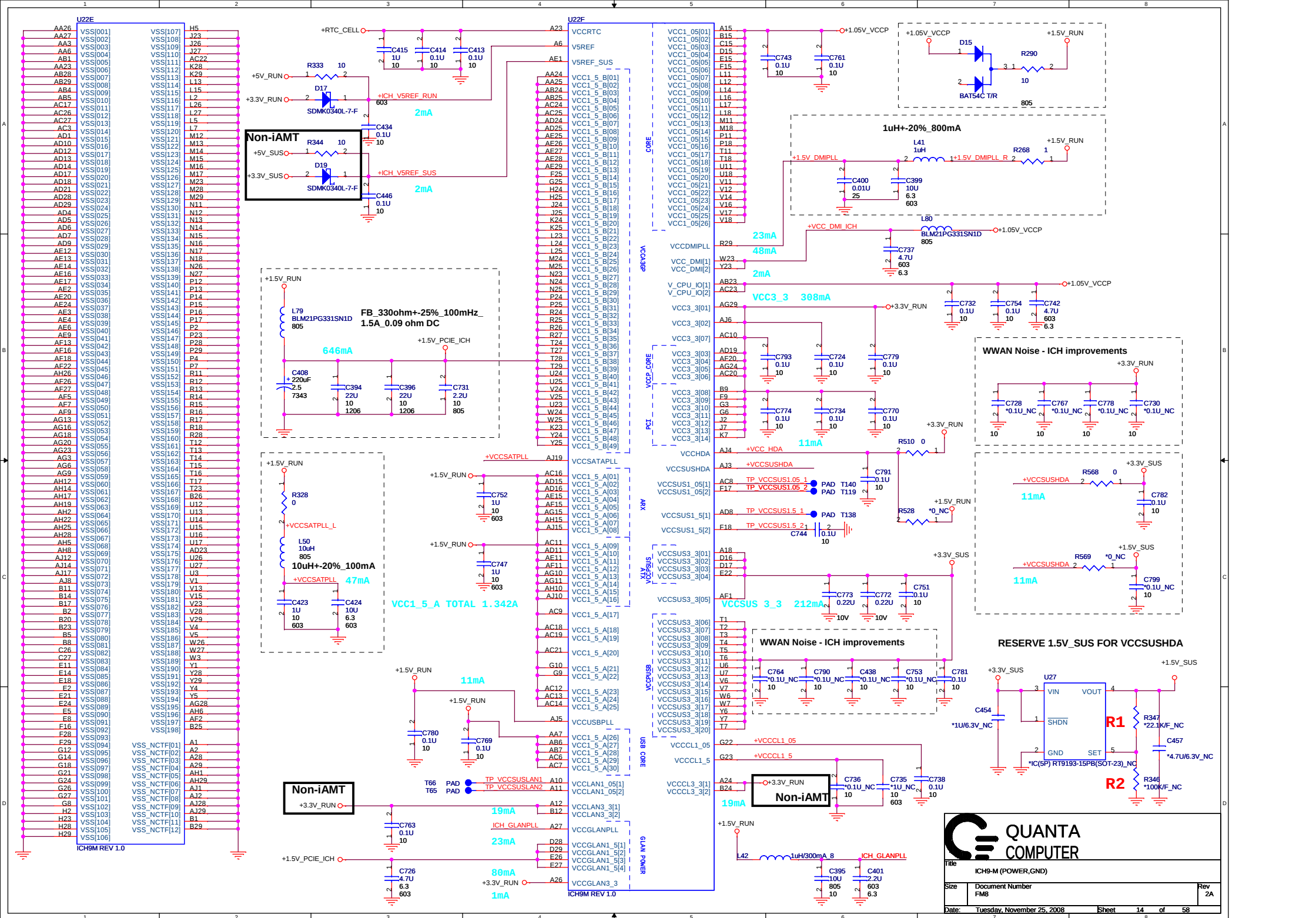


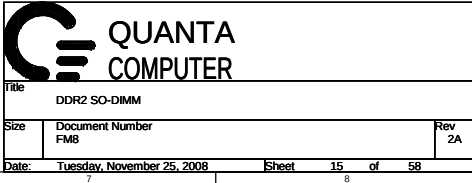
XOR Chain Entrance Strap		
ICH_RSVD	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

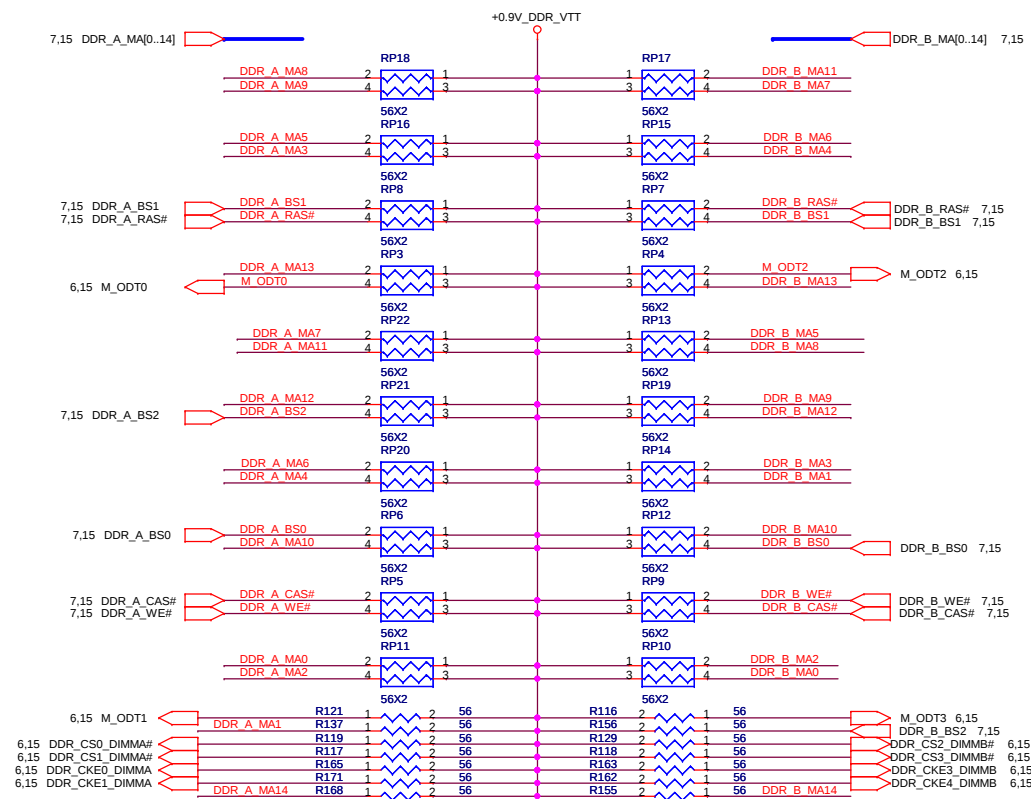
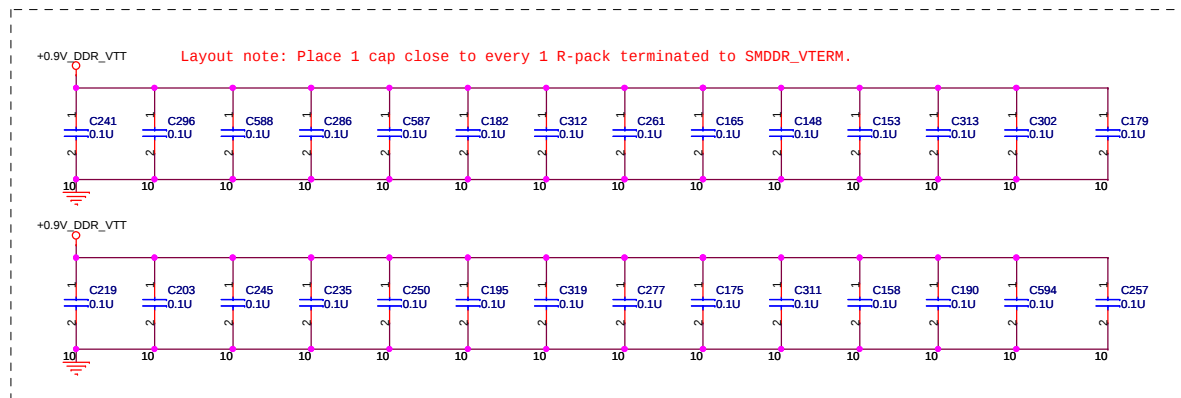


Title	ICH9-M (USB,DMI,PCIE,PCI)		
Size	Document Number FM8		R
Date:	Tuesday, November 25, 2008	Sheet	12 of 58





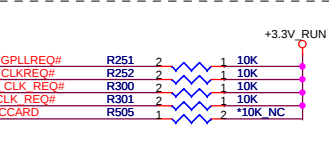
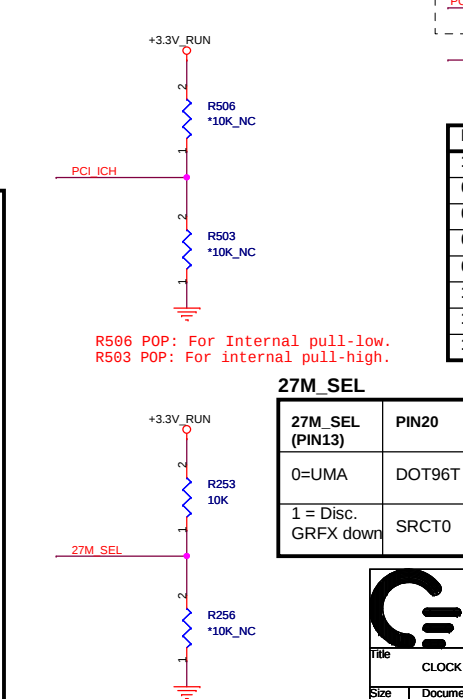
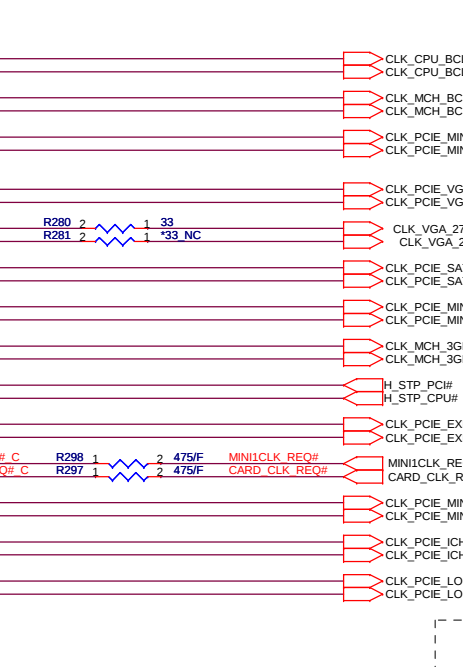
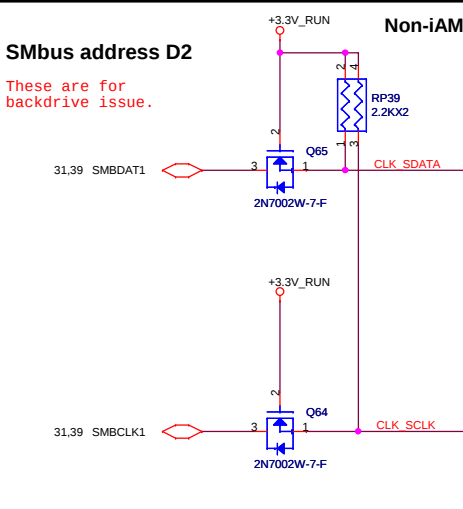
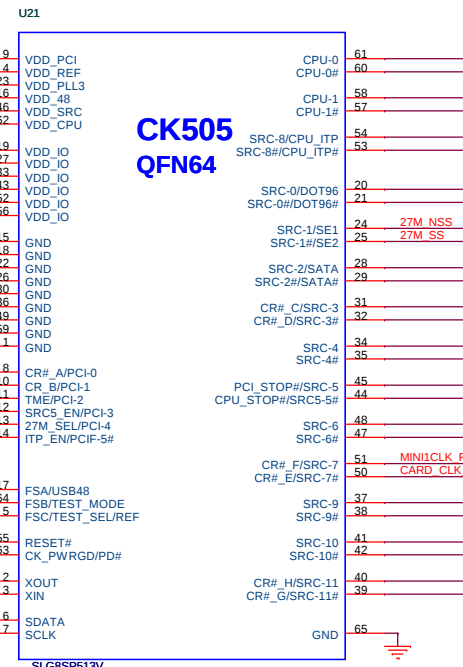
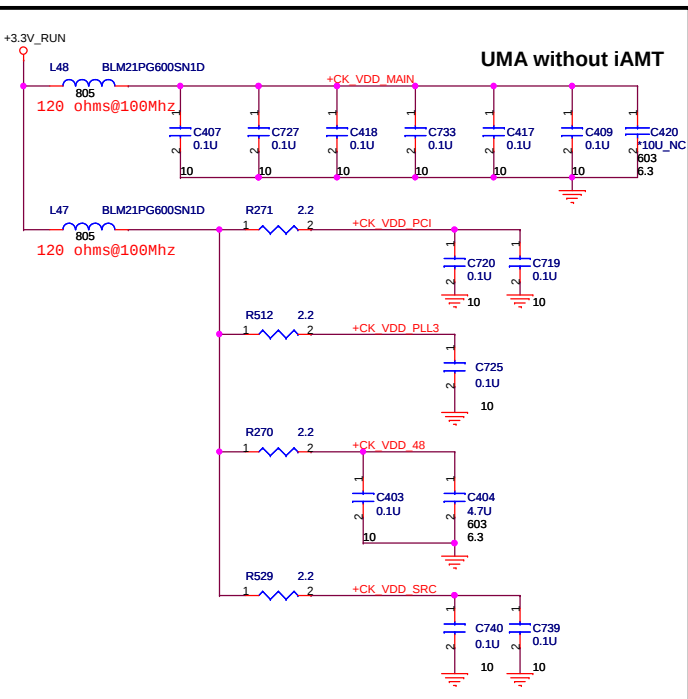
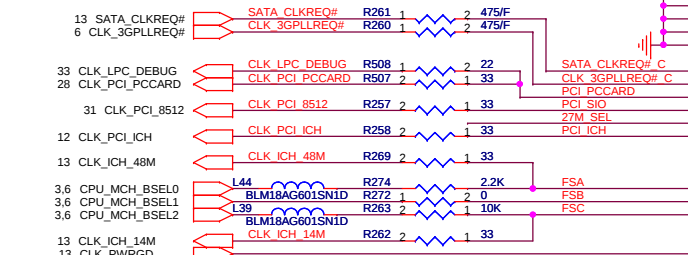
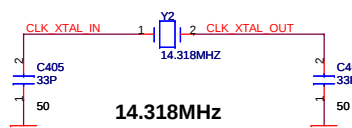
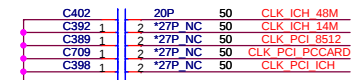




Layout notice:
Please these resistor
closely DIMMA,all
trace length<750 mil.

Layout notice:
Please these resistor
closely DIMMB,all
trace length<750 mil.

Add capacitor pads for improving WWAN.



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/100M_T	96/100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout



6 PCIE_MTX_GRX_P0[0..15]
6 PCIE_MTX_GRX_N0[0..15]

PCIE_MTX_GRX_P0 AE30
PCIE_MTX_GRX_N0 AE31
PCIE_MTX_GRX_P1 AE29
PCIE_MTX_GRX_N1 AD28
PCIE_MTX_GRX_P2 AD30
PCIE_MTX_GRX_N2 AC31
PCIE_MTX_GRX_P3 AC29
PCIE_MTX_GRX_N3 AB28
PCIE_MTX_GRX_P4 AB30
PCIE_MTX_GRX_N4 AA31
PCIE_MTX_GRX_P5 AA29
PCIE_MTX_GRX_N5 Y28
PCIE_MTX_GRX_P6 Y30
PCIE_MTX_GRX_N6 W31
PCIE_MTX_GRX_P7 W28
PCIE_MTX_GRX_N7 V28
PCIE_MTX_GRX_P8 V30
PCIE_MTX_GRX_N8 U31
PCIE_MTX_GRX_P9 U29
PCIE_MTX_GRX_N9 T28
PCIE_MTX_GRX_P10 T30
PCIE_MTX_GRX_N10 R31
PCIE_MTX_GRX_P11 R29
PCIE_MTX_GRX_N11 P28
PCIE_MTX_GRX_P12 P30
PCIE_MTX_GRX_N12 N31
PCIE_MTX_GRX_P13 N29
PCIE_MTX_GRX_N13 M28
PCIE_MTX_GRX_P14 M30
PCIE_MTX_GRX_N14 L31
PCIE_MTX_GRX_P15 L29
PCIE_MTX_GRX_N15 K30

U32A

PART 1 OF 10

PCI-EXPRESS INTERFACE

PCIE_RX0P AH30
PCIE_RX0N AG31
PCIE_RX1P AG29
PCIE_RX1N AF28
PCIE_RX2P AF27
PCIE_RX2N AF26
PCIE_RX3P AD27
PCIE_RX3N AD26
PCIE_RX4P AC25
PCIE_RX4N AB25
PCIE_RX5P Y23
PCIE_RX5N Y24
PCIE_RX6P AB27
PCIE_RX6N AB26
PCIE_RX7P Y27
PCIE_RX7N Y26
PCIE_RX8P W24
PCIE_RX8N W23
PCIE_RX9P V27
PCIE_RX9N U26
PCIE_RX10P U24
PCIE_RX10N U23
PCIE_RX11P T26
PCIE_RX11N T27
PCIE_RX12P T24
PCIE_RX12N T23
PCIE_RX13P P27
PCIE_RX13N P26
PCIE_RX14P P24
PCIE_RX14N P23
PCIE_RX15P M27
PCIE_RX15N M26

6 PCIE_MRX_GTX_P0[0..15]
6 PCIE_MRX_GTX_N0[0..15]

PCIE_MRX_GTX_P0 0.1U 2 1 C814 10 PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1 0.1U 2 1 C815 10 PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2 0.1U 2 1 C816 10 PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3 0.1U 2 1 C817 10 PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4 0.1U 2 1 C818 10 PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5 0.1U 2 1 C819 10 PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6 0.1U 2 1 C820 10 PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7 0.1U 2 1 C821 10 PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8 0.1U 2 1 C822 10 PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9 0.1U 2 1 C823 10 PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10 0.1U 2 1 C824 10 PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11 0.1U 2 1 C825 10 PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12 0.1U 2 1 C826 10 PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13 0.1U 2 1 C827 10 PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14 0.1U 2 1 C828 10 PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15 0.1U 2 1 C829 10 PCIE_MRX_GTX_C_P15
PCIE_MRX_GTX_N0 0.1U 2 1 C830 10 PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1 0.1U 2 1 C831 10 PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2 0.1U 2 1 C832 10 PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3 0.1U 2 1 C833 10 PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4 0.1U 2 1 C834 10 PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5 0.1U 2 1 C835 10 PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6 0.1U 2 1 C836 10 PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7 0.1U 2 1 C837 10 PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8 0.1U 2 1 C838 10 PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9 0.1U 2 1 C839 10 PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10 0.1U 2 1 C840 10 PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11 0.1U 2 1 C841 10 PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12 0.1U 2 1 C842 10 PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13 0.1U 2 1 C843 10 PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14 0.1U 2 1 C844 10 PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15 0.1U 2 1 C845 10 PCIE_MRX_GTX_C_N15

100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing.
Clock must be provided less than 400ns
after CLKREQ# is asserted

17 CLK_PCIE_VGA AK30
17 CLK_PCIE_VGA# AK32
13 PLTRST_DELAY# AL27
6,12,30,31,33,34,42 PLTRST# M92-S2/M92-XT

43

(1.1V)
+PCIE_VDDC

M92-S2 XT AJ072800T04 100-C61675(216-0728004)
M92-S2 AJ072800T03 100-C61643(216-0728003)

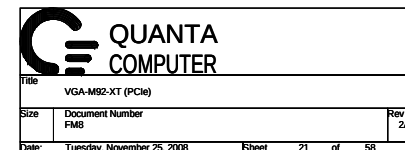


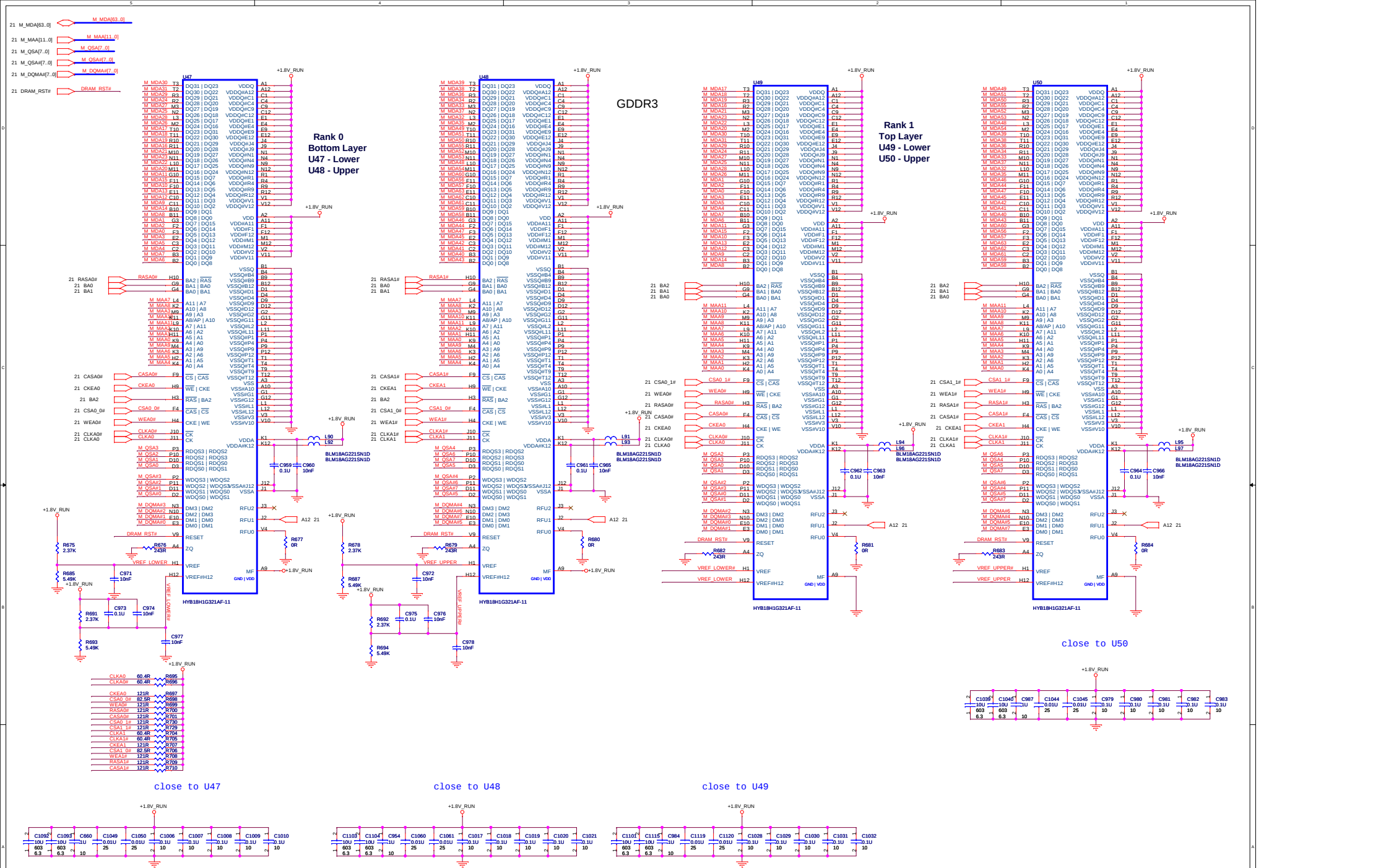
Title		
VGA-M92-XT (PCIe)		
Size	Document Number FM8	Rev 2A
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U32C

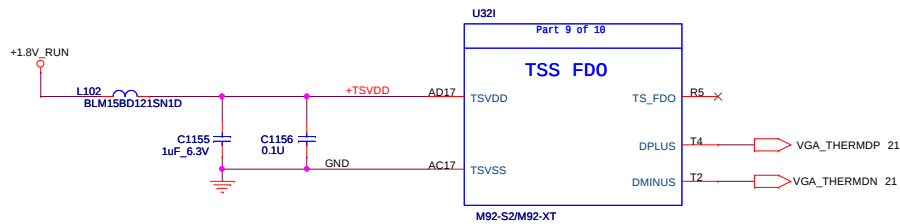
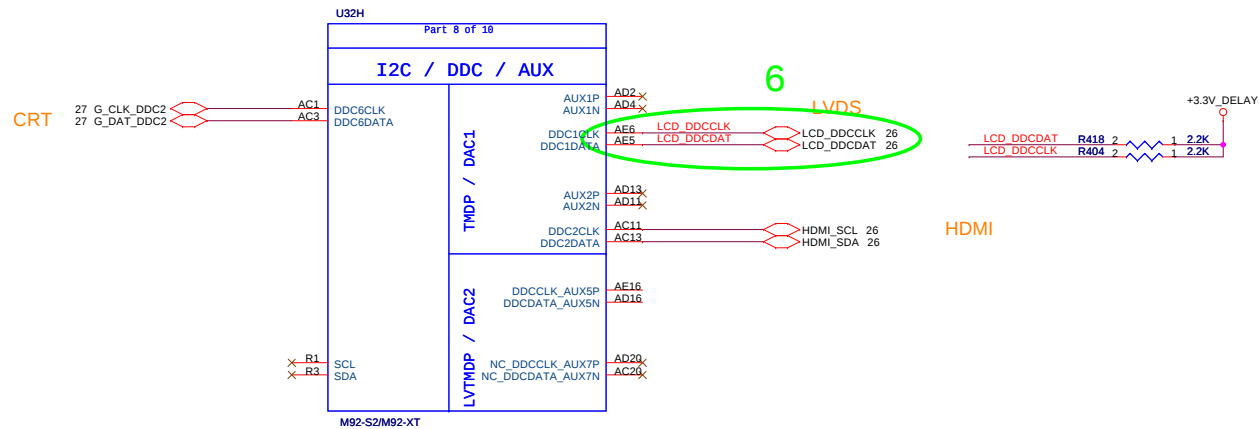
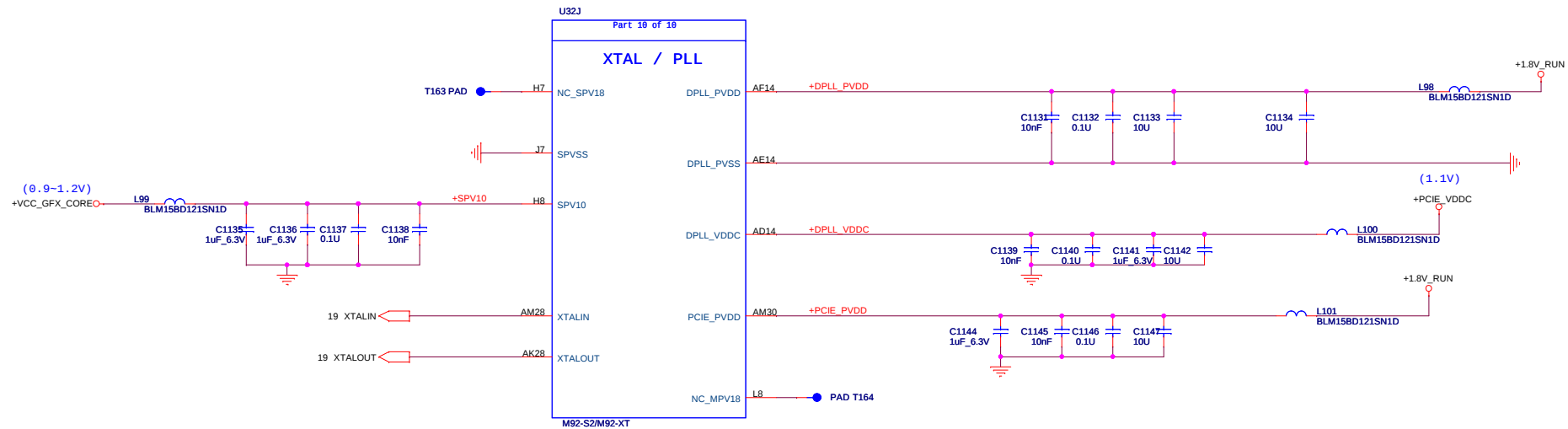


THERMAL MONITOR

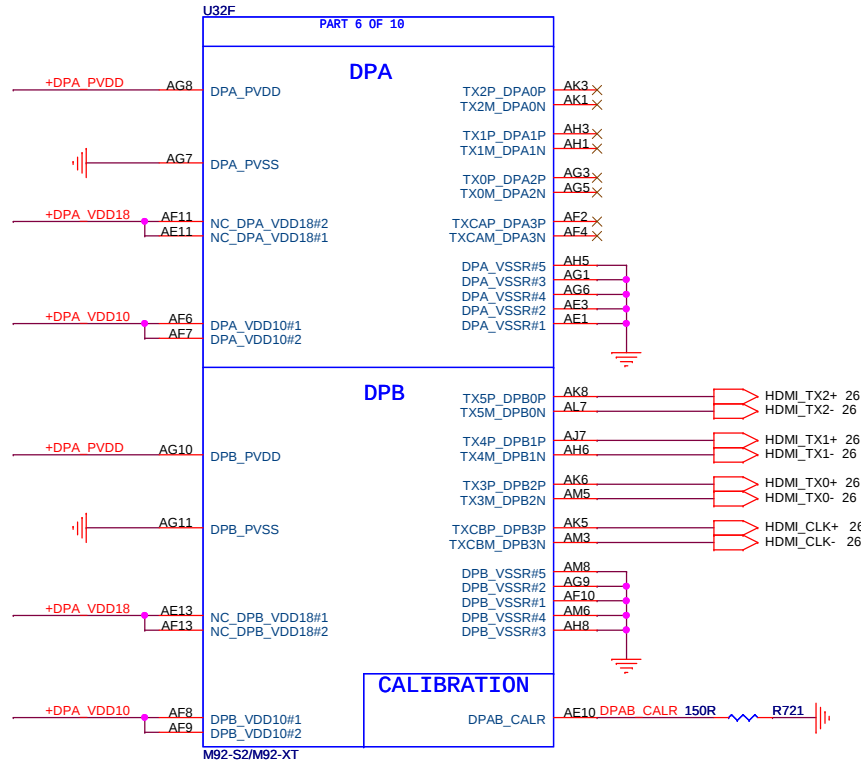




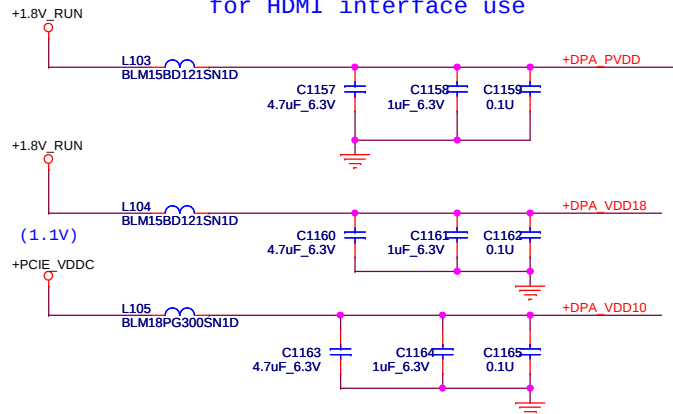
Base on M82 GDDR Caps.



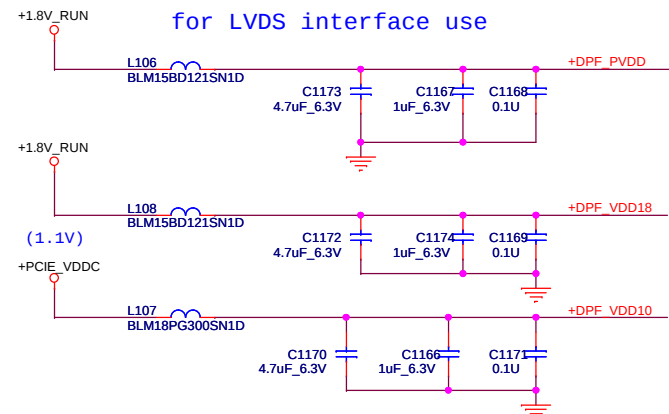
TMDP(HDMI) INTERFACE



for HDMI interface use



for LVDS interface use



Title			VGA-M92-XT (PCIe)
Size	Document Number	Rev	
	FM8	2A	
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Title	Author	Year	Journal	Volume	Page
1. The Effect of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	1-15
2. The Impact of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	16-30
3. The Effect of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	31-45
4. The Impact of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	46-60
5. The Effect of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	61-75
6. The Impact of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	76-90
7. The Effect of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	91-105
8. The Impact of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	106-120
9. The Effect of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	121-135
10. The Impact of the 1997 Asian Crisis on the U.S. Economy	John H. Coatsworth	1998	Journal of International Economics	50	136-150

VGA-M82-S (PCIe)

Size

Document Number FM8

Rev
2/

Date:

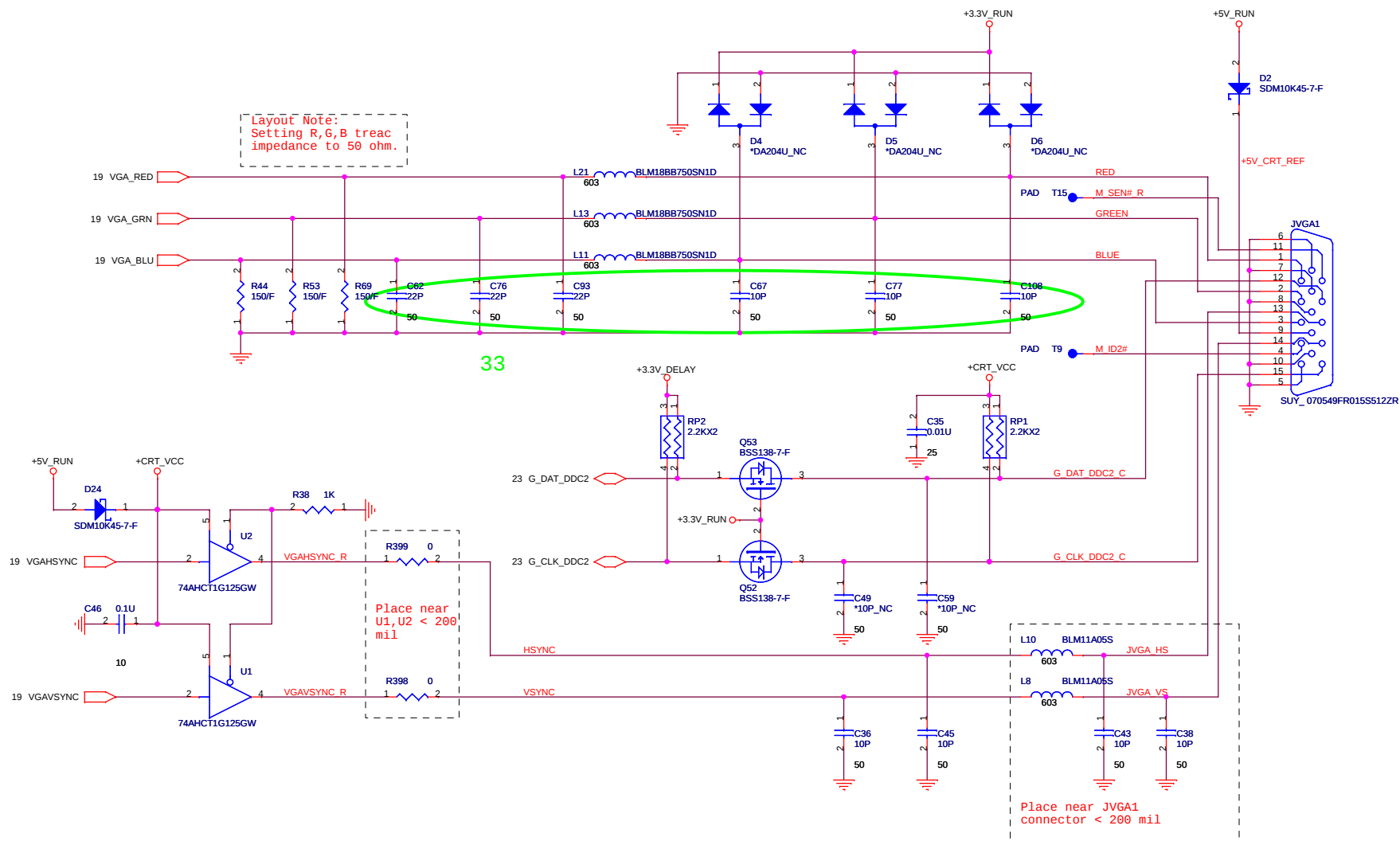
Tuesday, November 25, 2008

Sheet

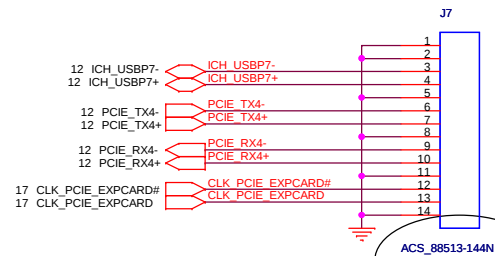
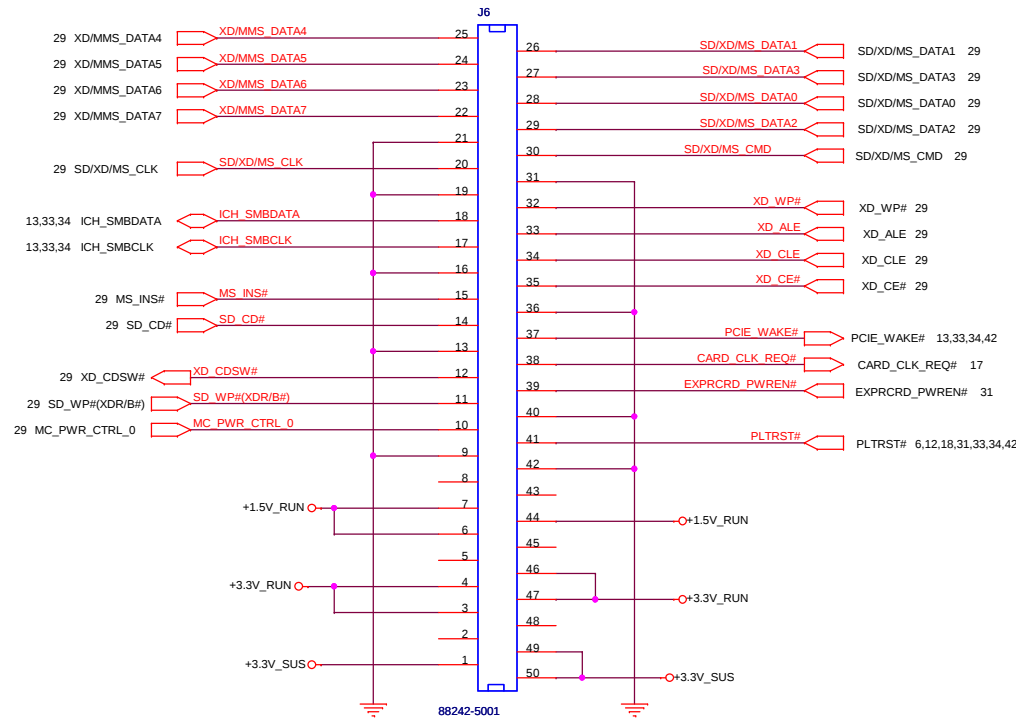
25

of

58

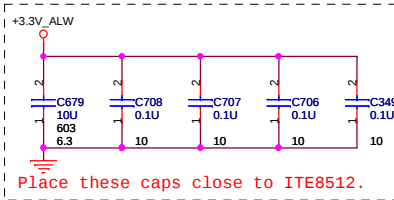


Express Card/CARD READER



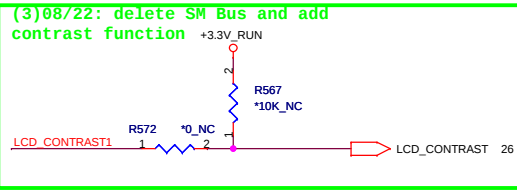
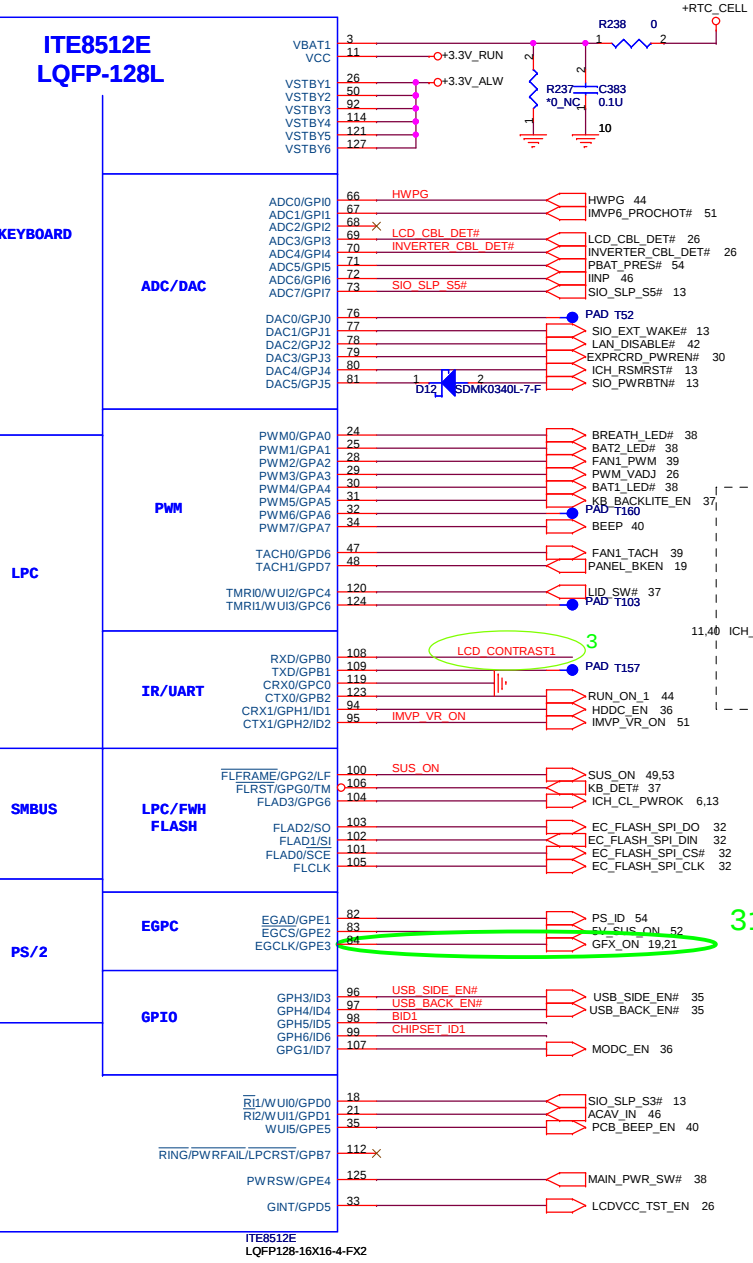
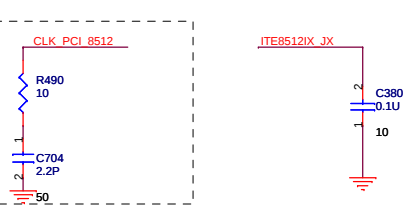
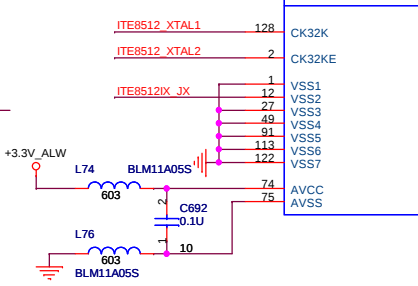
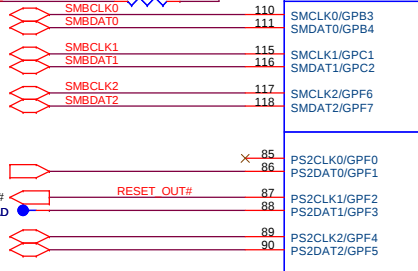
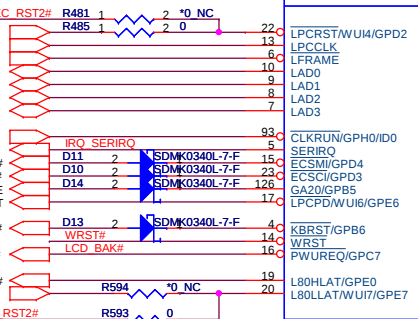
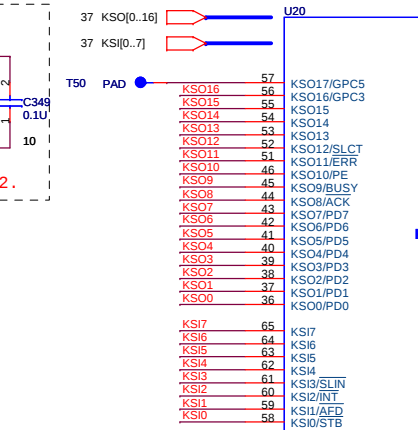
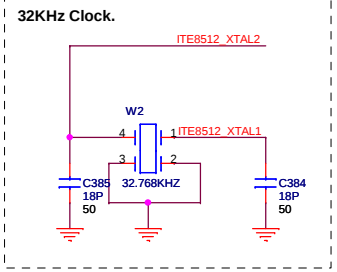
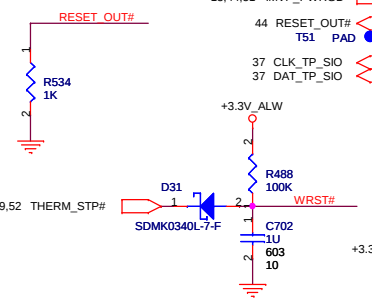
8/28:change PN to 88513-144N

QUANTA COMPUTER		
Title: ExpressCard/SmartCard		
Size:	Document Number: FM8	Rev: 2A
Date:	Tuesday, November 25, 2008	Sheet: 30 of 58

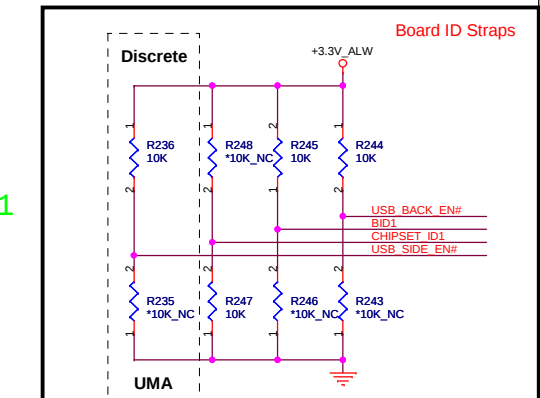
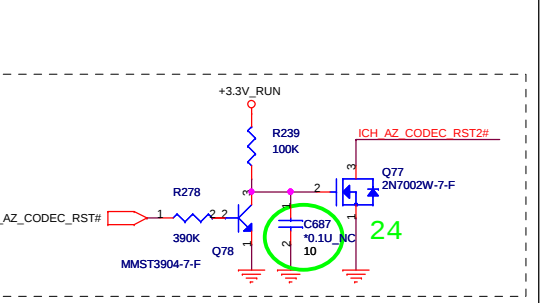
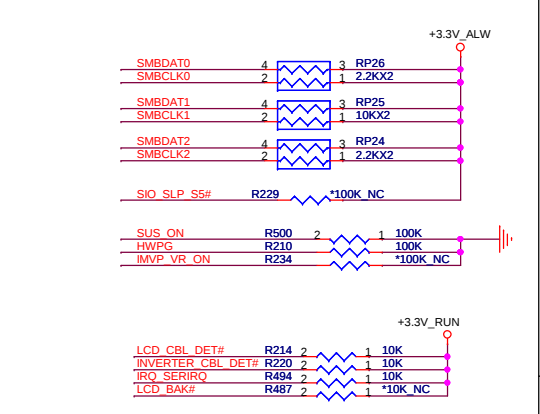


Place these caps close to ITE8512.

Charge and BAT
CLK, LCD and Thermal
G_Thermal
and Media button



(3)08/22: delete SM Bus and add contrast function



VGA_IDENTIFY

BID0

CHIPSET ID1	BID1	USB BACK_EN#	FM6B(UMA)	FM6(Ds)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	OT (A00)	OT (A00)
0	0	0	(A01)	(A01)
0	0	1		

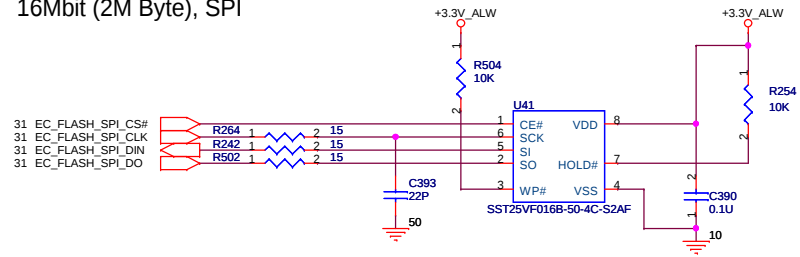
QUANTA COMPUTER

Ultra iVO Controller ECE5028

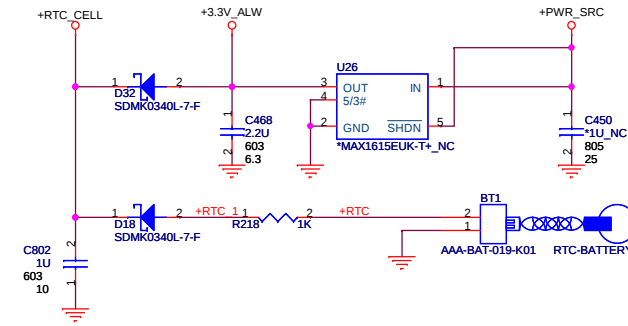
Size: Document Number: FMB8 Rev: 2A

Date: Tuesday, November 25, 2008 Sheet: 31 of 58

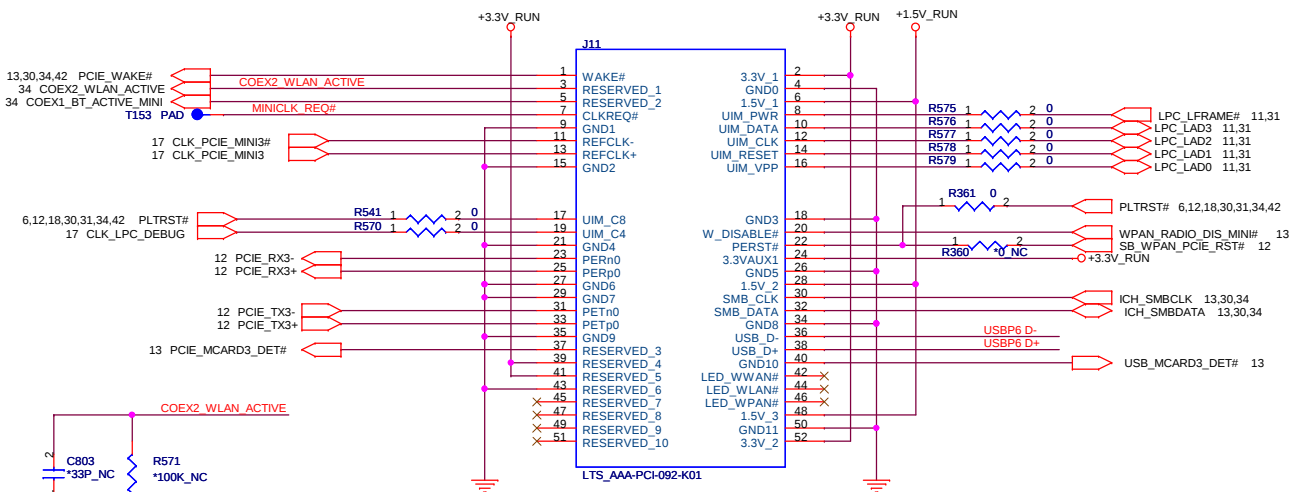
16Mbit (2M Byte), SPI



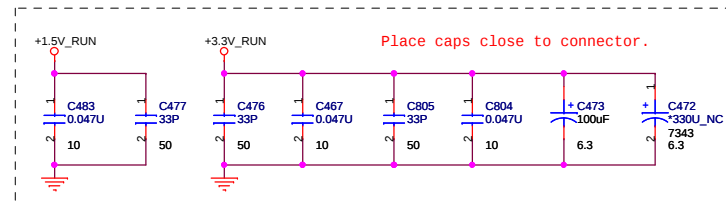
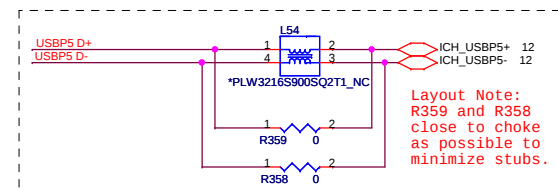
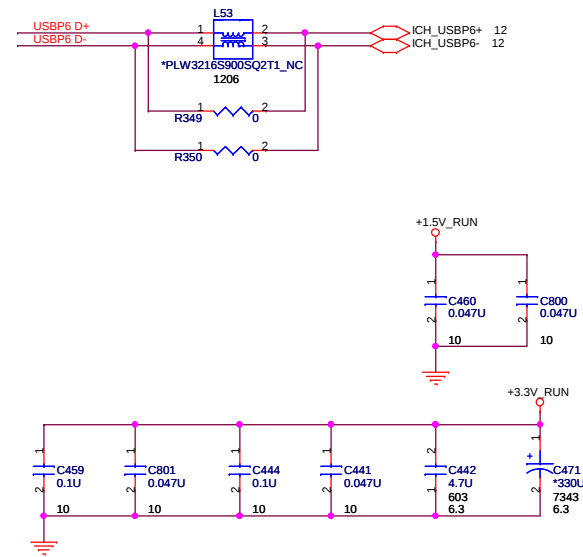
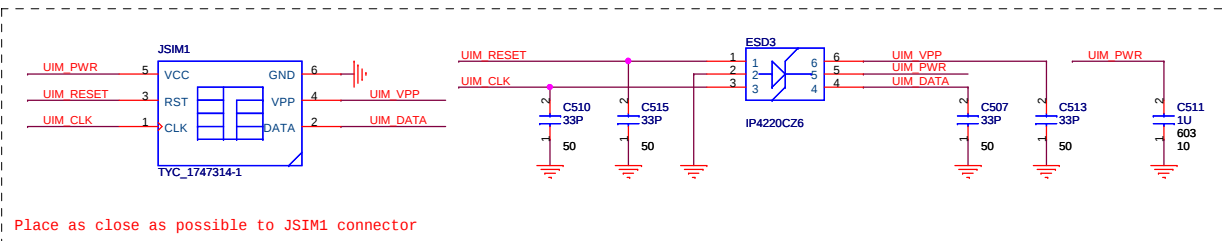
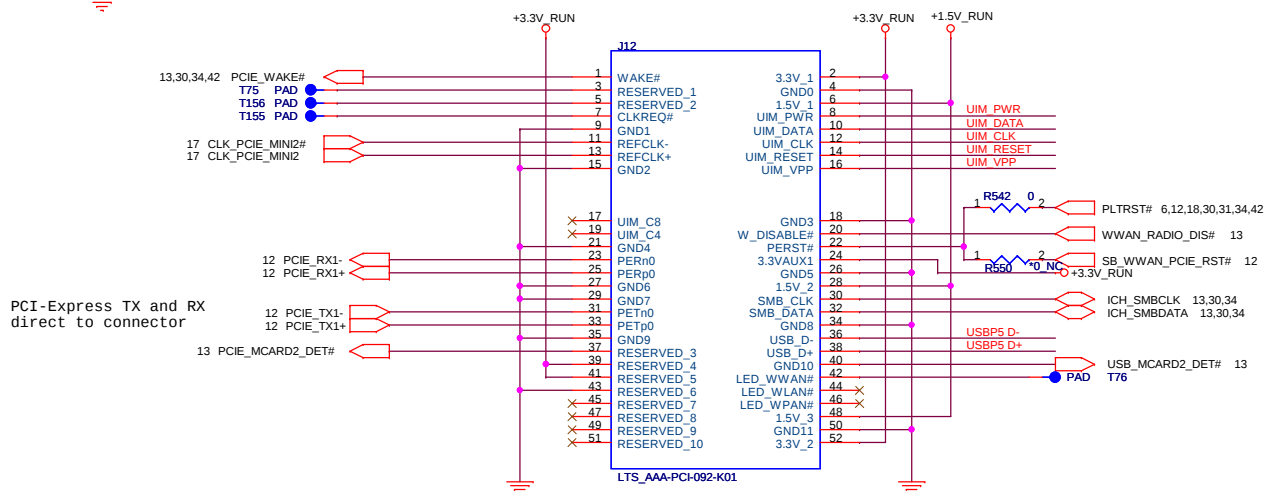
RTC BATTERY



MiniCard Robson, BT. UWB connector



MiniCard WWAN connector



Title

MINI-PCI

Size

Document Number

Rev

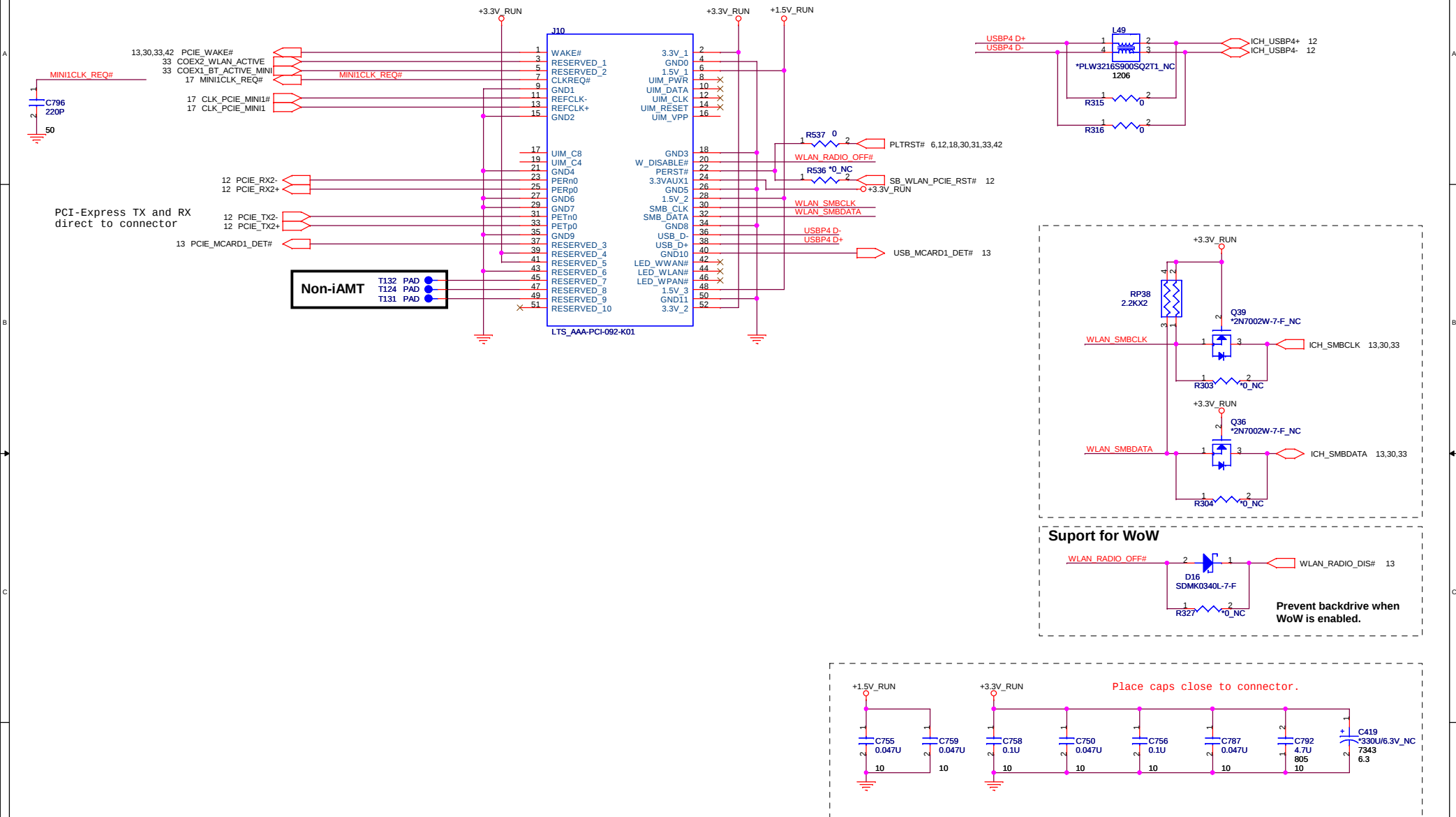
Date: Tuesday, November 25, 2008

Sheet

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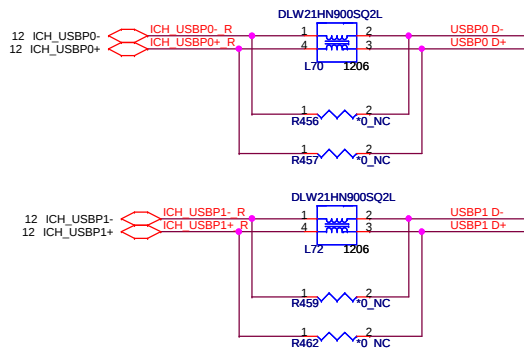
58

MiniCard WLAN connector



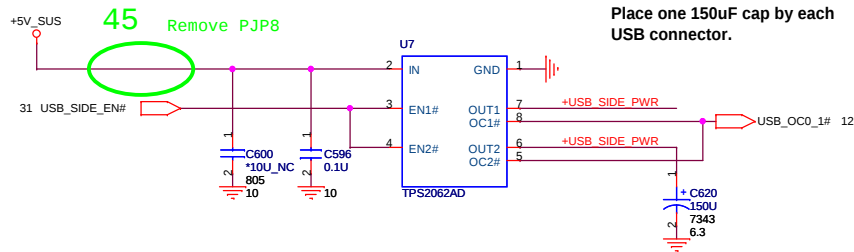
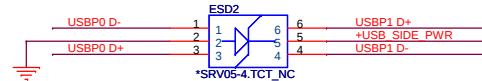
Title			MDC CONN.
Size	Document Number	Rev	
FMS		2A	
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External USB PORT hookup reference. Your design may need more or less external ports and may be mapped differently

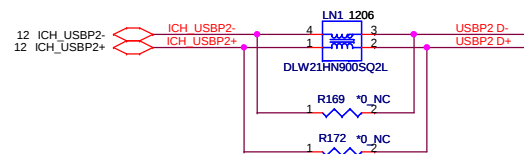


Platforms should put in PADS for the USB chokes if they have the room. Chokes should be NOPOP.

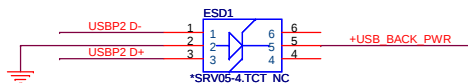
Place ESD diodes as close as USB connector.



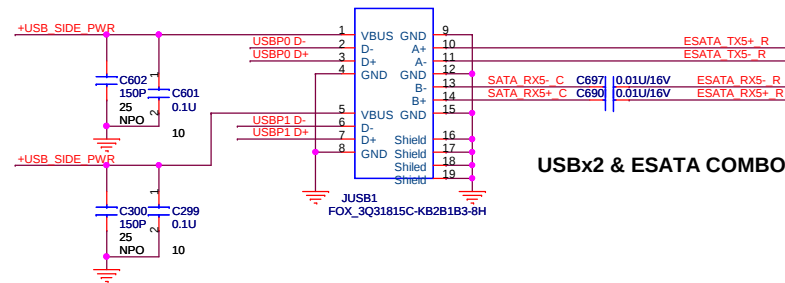
Place one 150uF cap by each USB connector.



Place ESD diodes as close as USB connector.

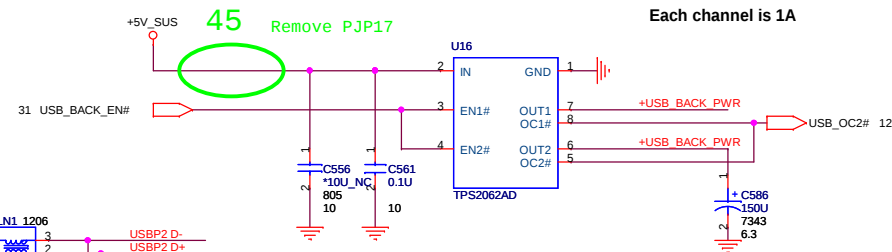
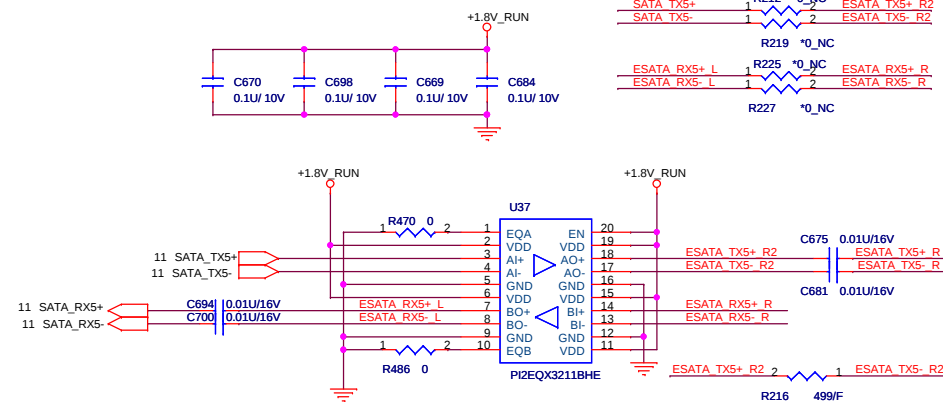


Side External USB2

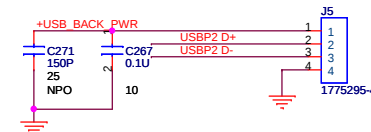


USB2 & ESATA COMBO

E-SATA Re-driver

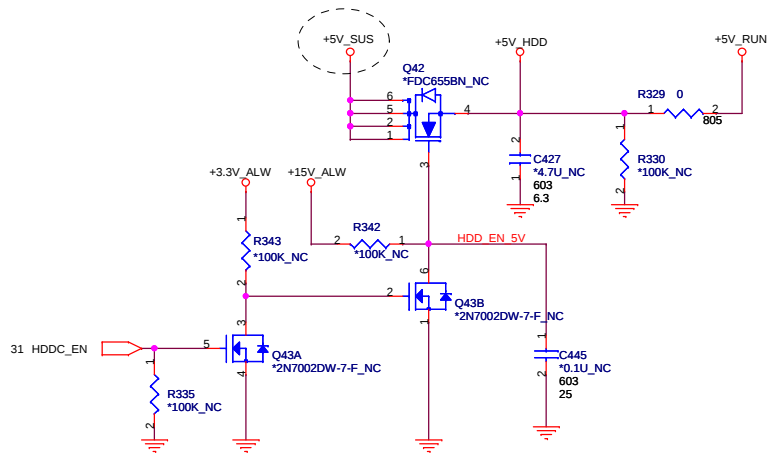
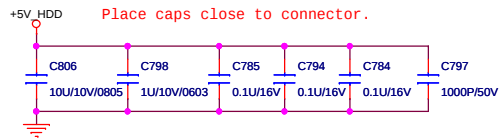
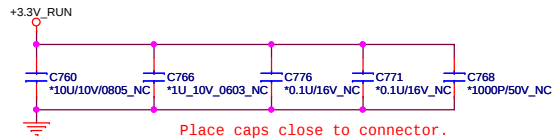
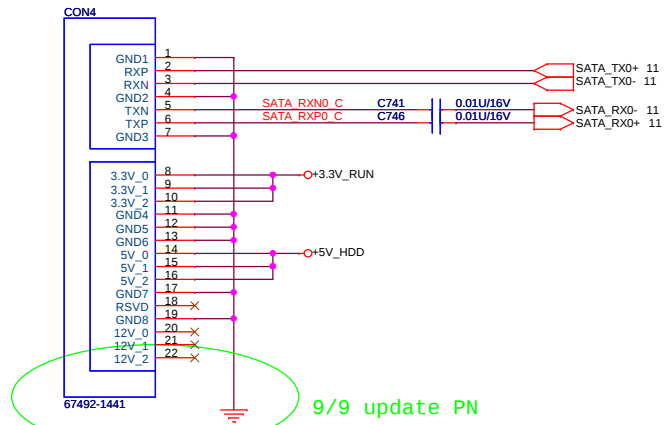


Each channel is 1A

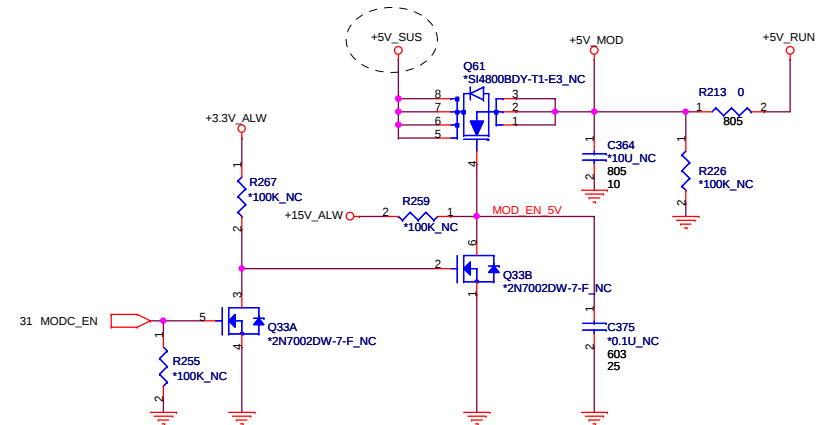
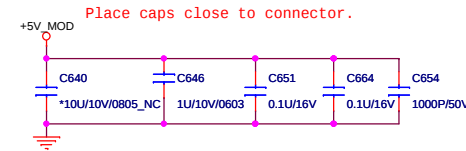
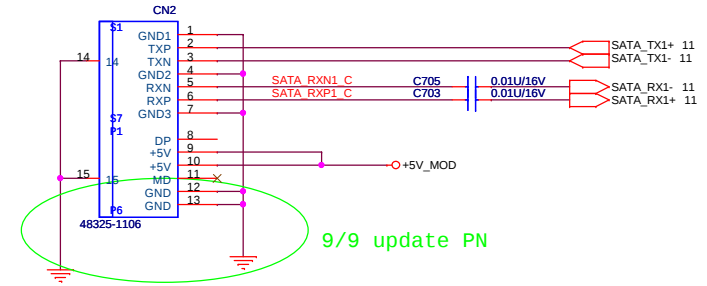


Title			SERIAL PORT & USB
Size	Document Number	Rev	
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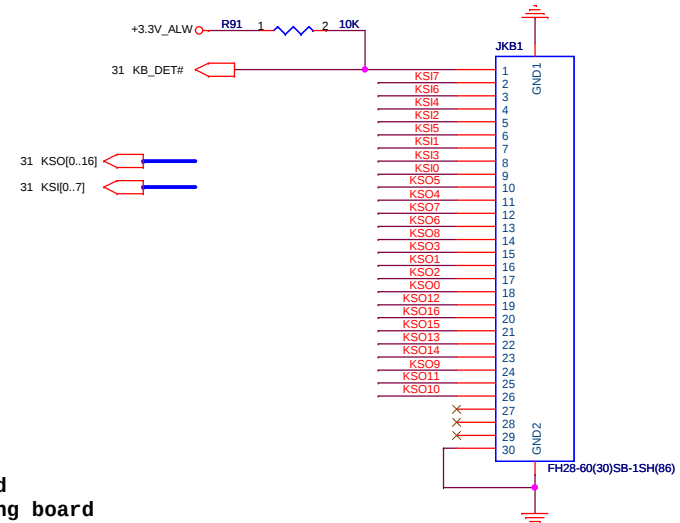
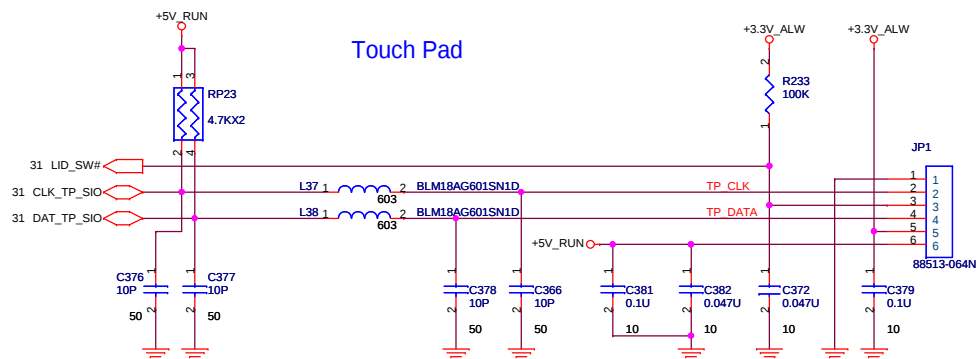
SATA Connector.



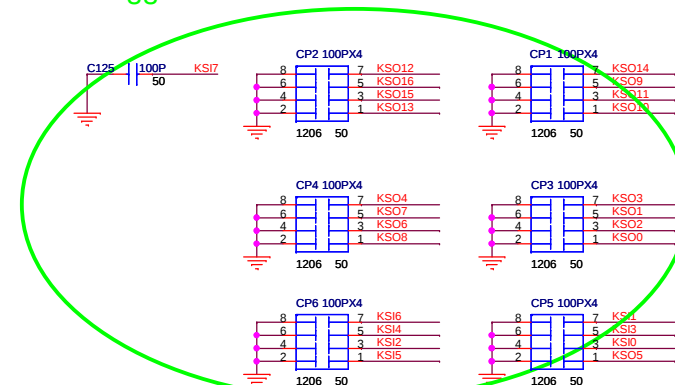
ODD Connector



Title			SATA (HDD&CD_ROM)
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	FMB	2A	
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100P CAPS CLOSE TO JKB1

The schematic diagram illustrates the LED driver circuit for the QUANTA COMPUTER TOUCH PAD, BULE TOOTH & FIR. The circuit is powered by three input signals: +3.3V_ALW, +15V_ALW, and +5V_RUN. The +3.3V_ALW signal is connected to the gate of MOSFET Q11B (2N7002DW-7-F_NC) through resistor R45 (100K_NC). The +15V_ALW signal is connected to the gate of MOSFET Q11A (2N7002DW-7-F_NC) through resistor R36 (100K_NC). The +5V_RUN signal is connected to the gate of MOSFET Q9 (Si2304BDS-T1-E3_NC) through resistor R42 (20K_NC). The output of the circuit is connected to the LED1 and LED2 pins of the 88513-044N component. The circuit includes two LEDs (LED1 and LED2) and various resistors (R45, R36, R42, R115, R105) and capacitors (C56, C37).

QUANTA
COMPUTER

Title	
TOUCH PAD, BULE TOOTH & FIR	
Size	Document Number



Title	TOUCH PAD, BULE TOOTH & FIR
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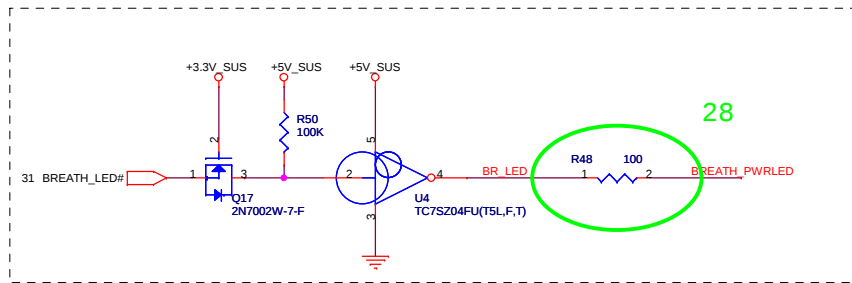
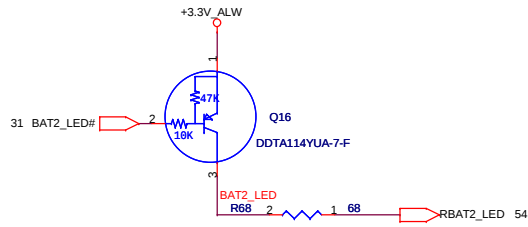
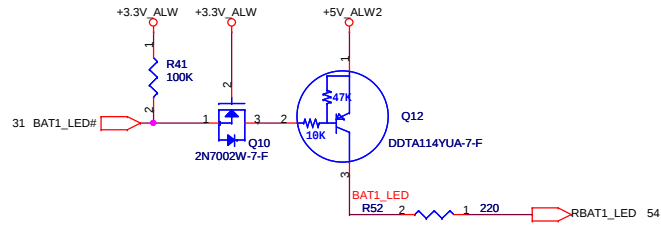
Size	Document Number
	EMB

Rev
2A

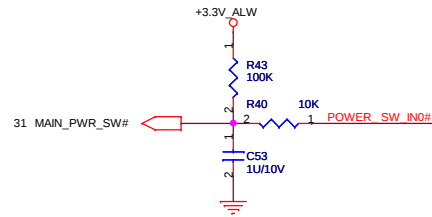
Date: Tuesday, November 25, 2008

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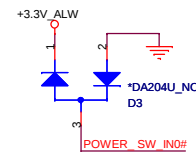
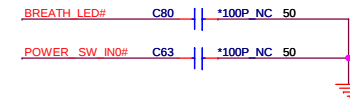
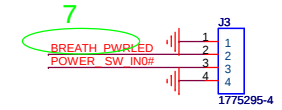
Battery status.

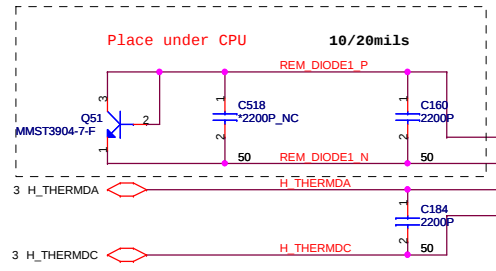
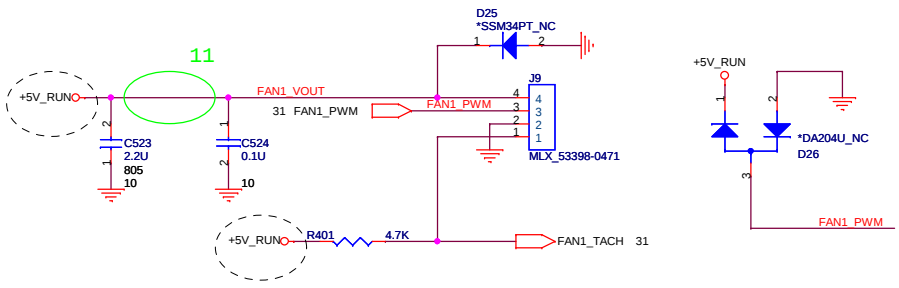


Power Switch

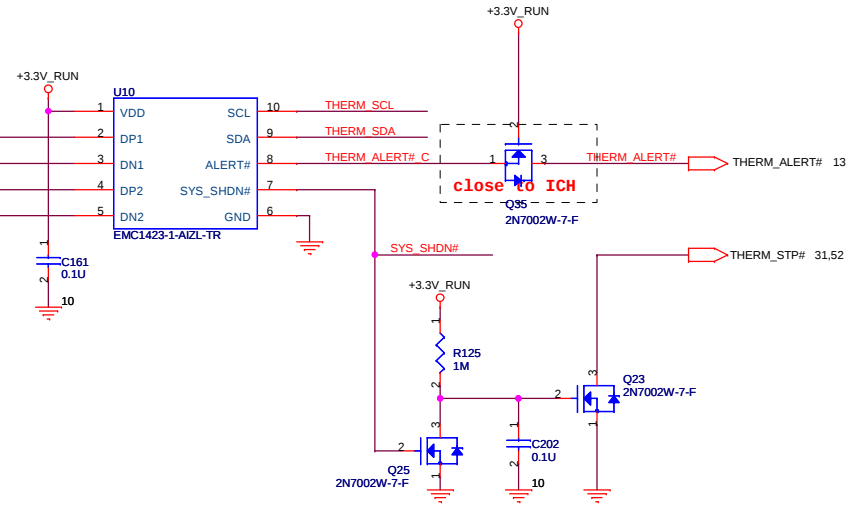
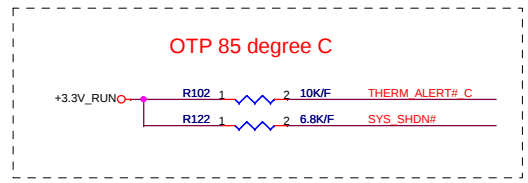
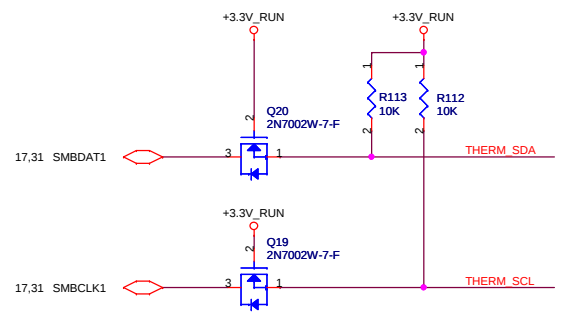


Power button cable

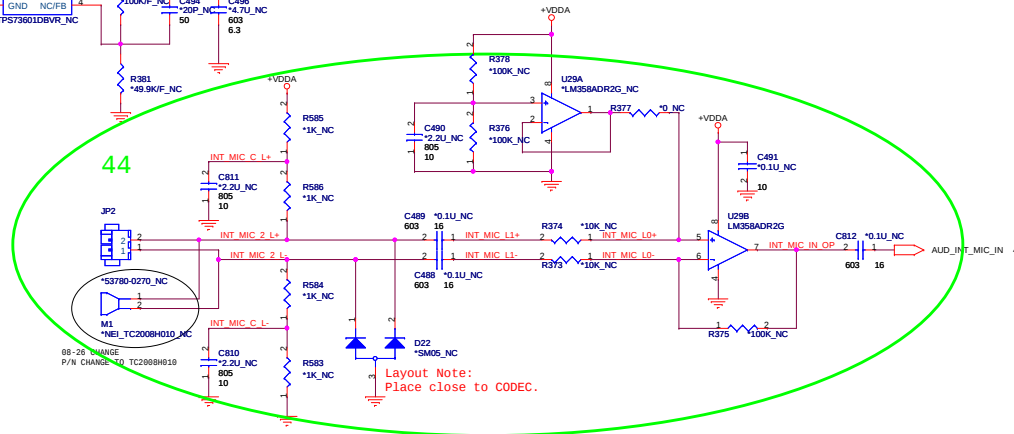
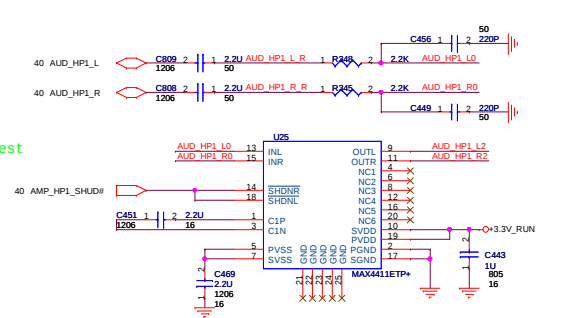
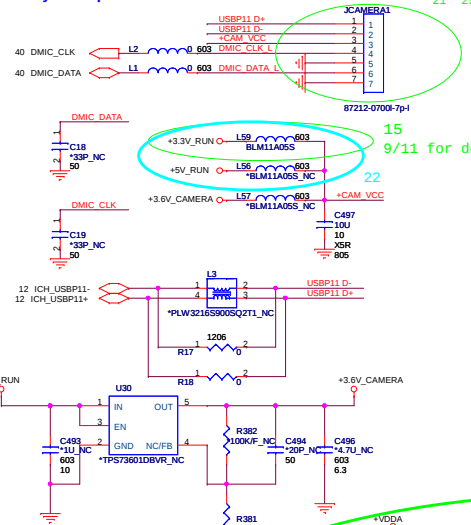
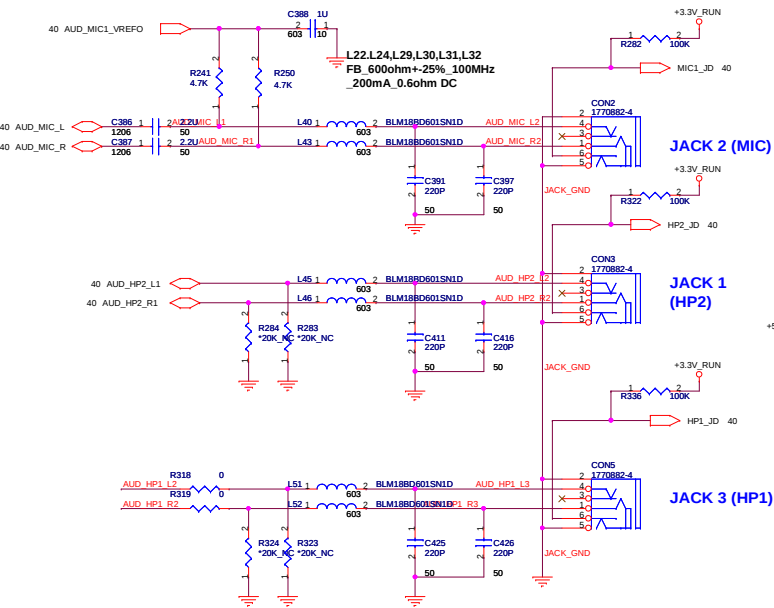




Cap should close to thermal IC

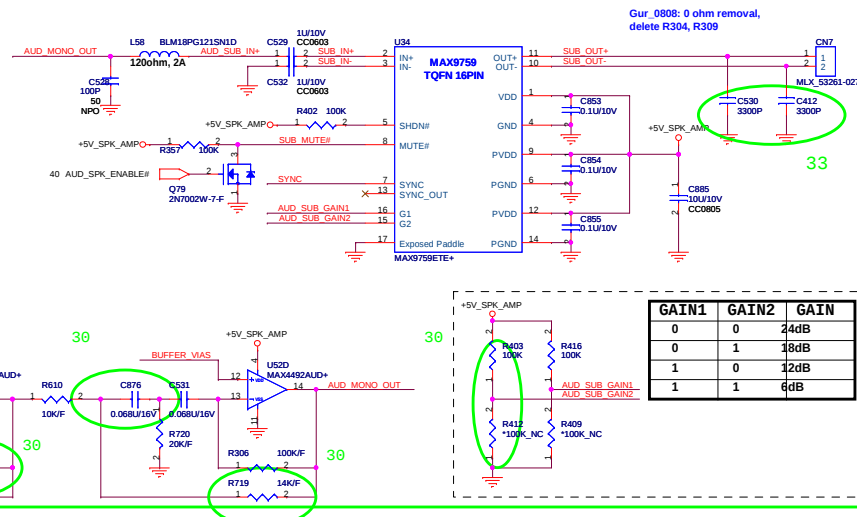


Headphone Jack
Stereo MIC Jack

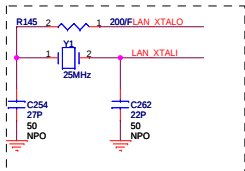
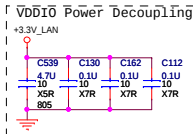
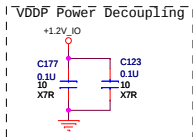
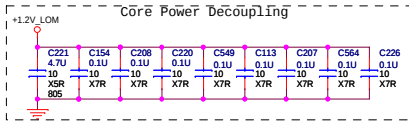


INTERNAL SUBWOOFER AMP

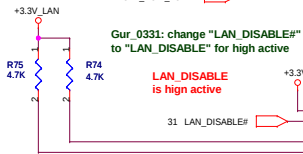
SYNC	Condition
VDD	Spread-spectrum mode with fS = 1200kHz $\pm$ 70kHz.
GND	Fixed-frequency mode with fS = 1100kHz.
FLOAT	Fixed-frequency mode with fS = 1500kHz.
Clocked	Fixed-frequency mode with fS = external clock frequency.



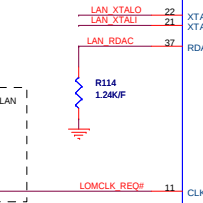
GAIN1	GAIN2	GAIN
0	0	24dB
0	1	18dB
1	0	12dB
1	1	6dB



12 PCIE_RX6+GLAN_RX+
12 PCIE_RX6+GLAN_RX-
12 PCIE_TX6+GLAN_TX+
12 PCIE_TX6+GLAN_TX-
13,30,33,34 PCIE_WAKE#
6,12,18,30,31,33,34 PLTRST#
12 SB_LOM_PCIE_RST#
17 CLK_PCIE_LOM#
17 CLK_PCIE_LOM#

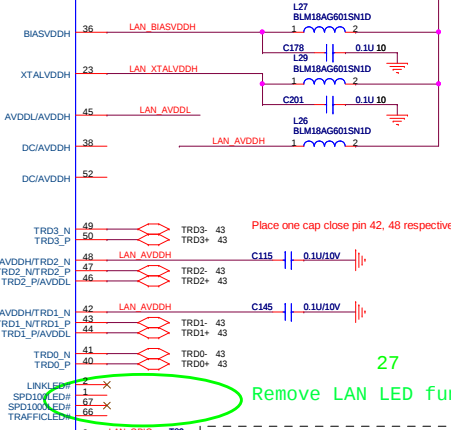


Make sure it stays high when not driven by BCM5784M.



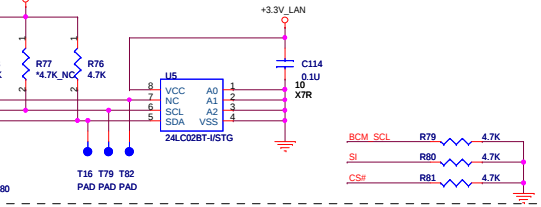
BCM5784M
10mm x 10mm
68-Pin QFN

U9



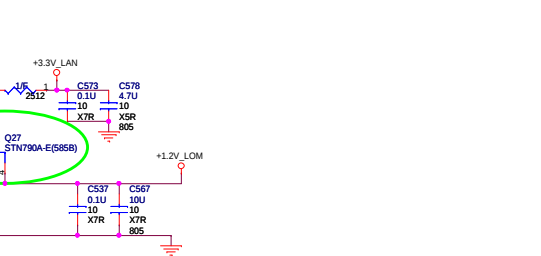
Remove LAN LED function

R78 & R76: Stuff only if U5 is installed



Remove LAN LED function

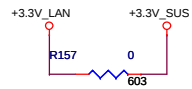
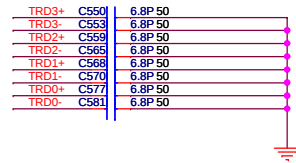
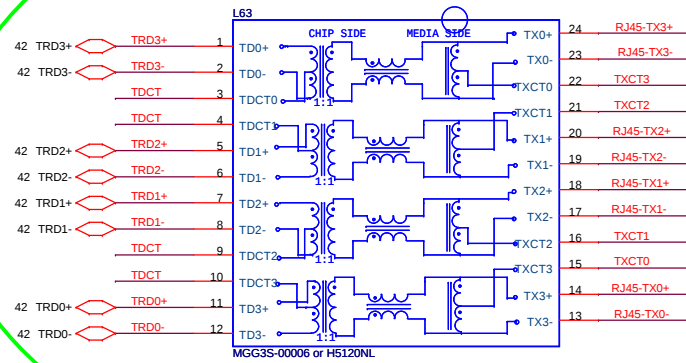
R78 & R76: Stuff only if U5 is installed



Note: thermal pad

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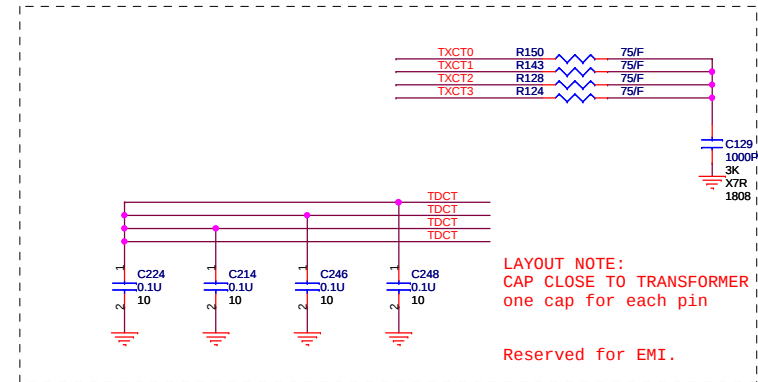
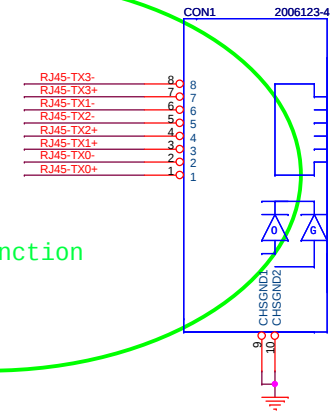
TRANSFORM



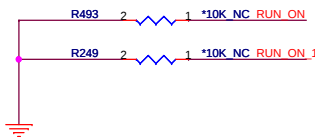
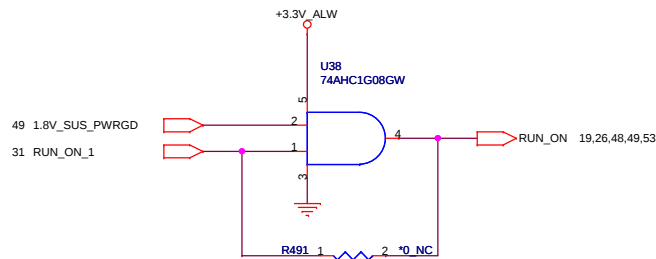
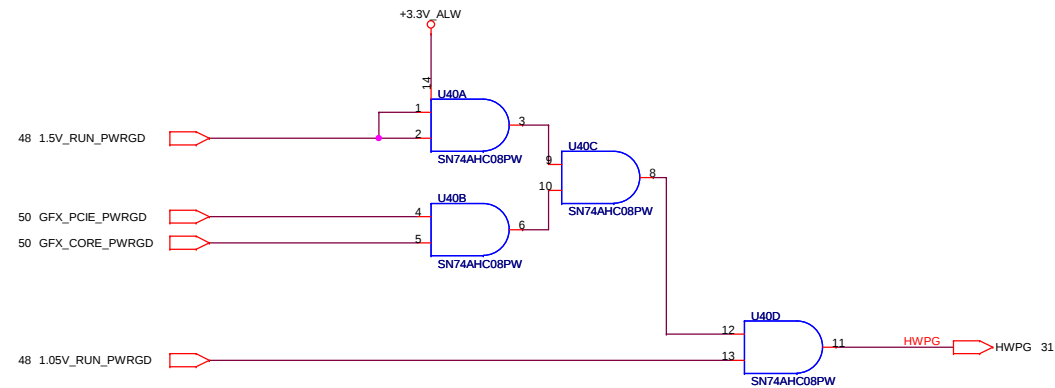
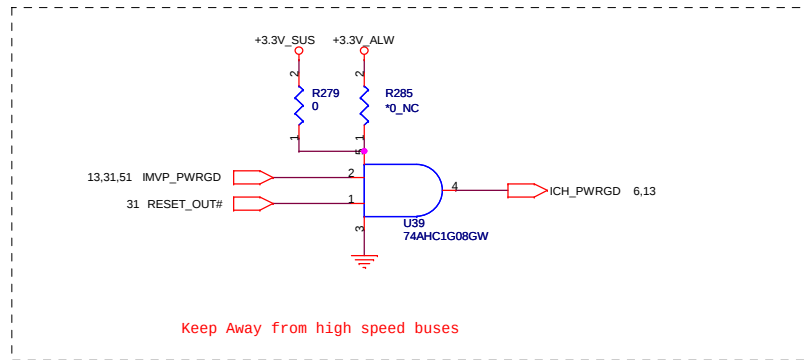
RJ-45 Connector

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Remove LAN LED function



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A					
B					
C					
D					

 QUANTA COMPUTER		
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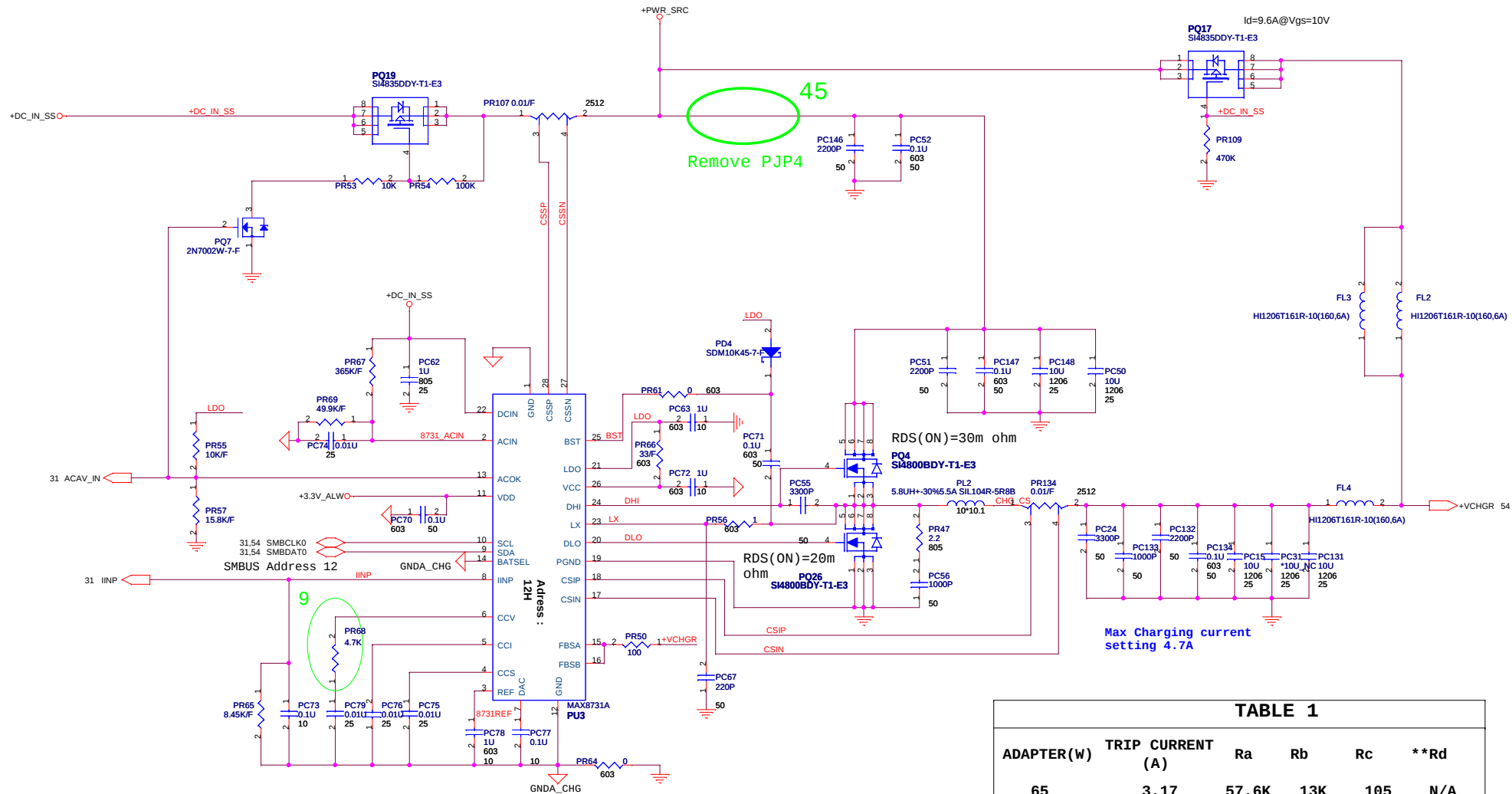


TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	Ra	Rb	Rc	**Rd
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.25 (see note3)	32.4K	6.49K	115	N/A

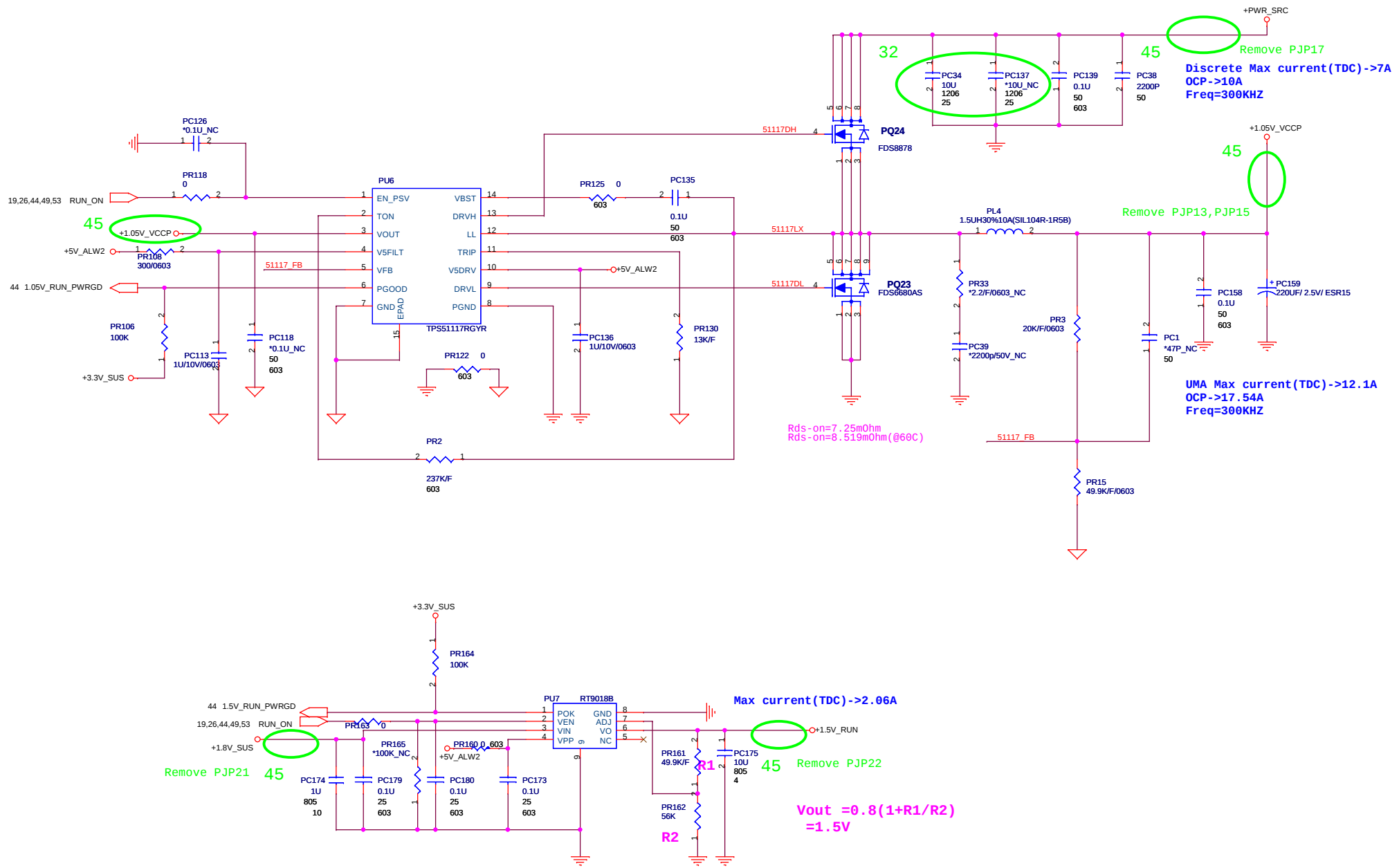
Note 1: PR96 is populated if ADAPT_TRIP_SEL is used to program for the next lower adaptor.
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

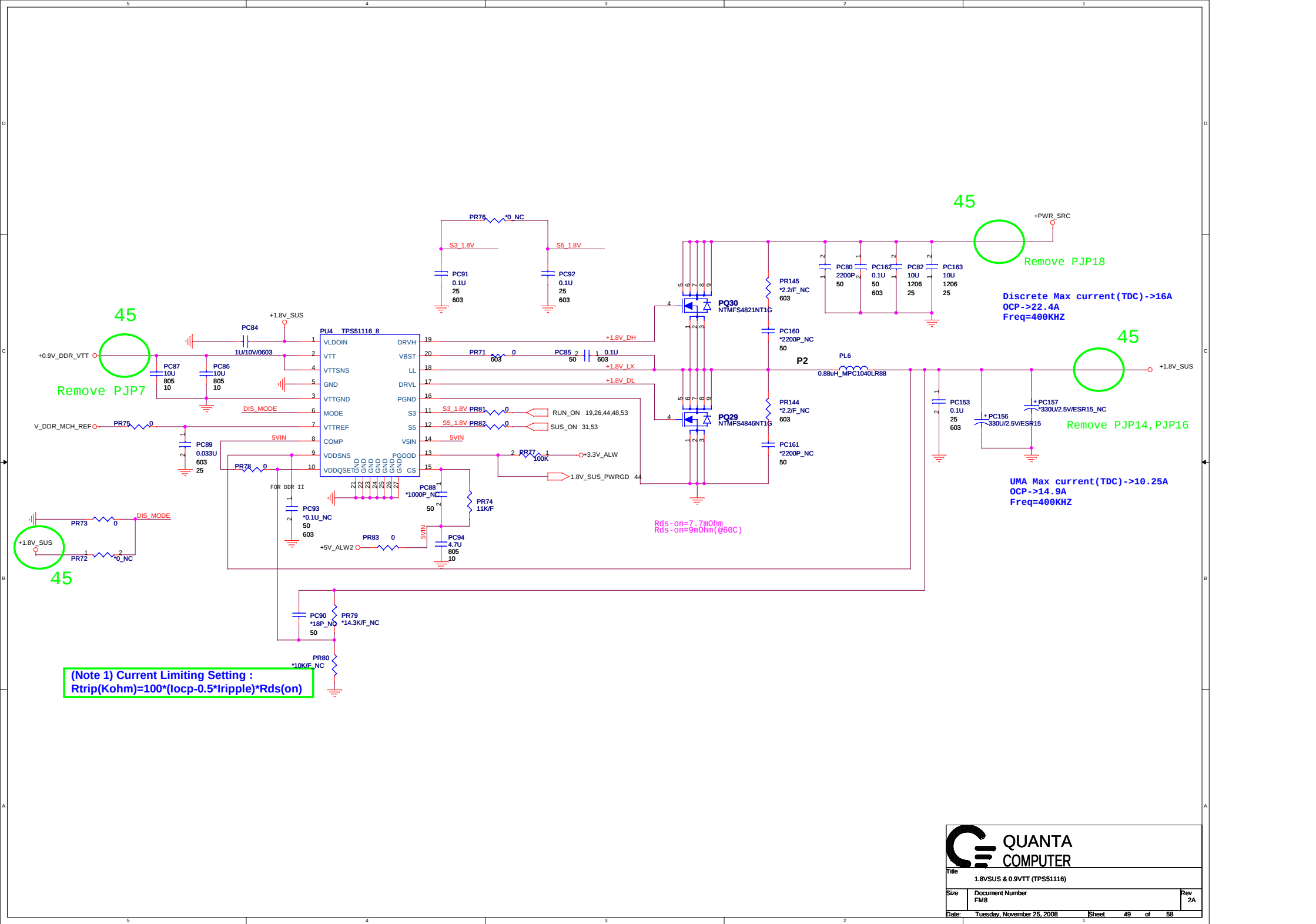
Note 2: 24.9K at PR96 allows the 65W adaptor setting to switch down to 45W.

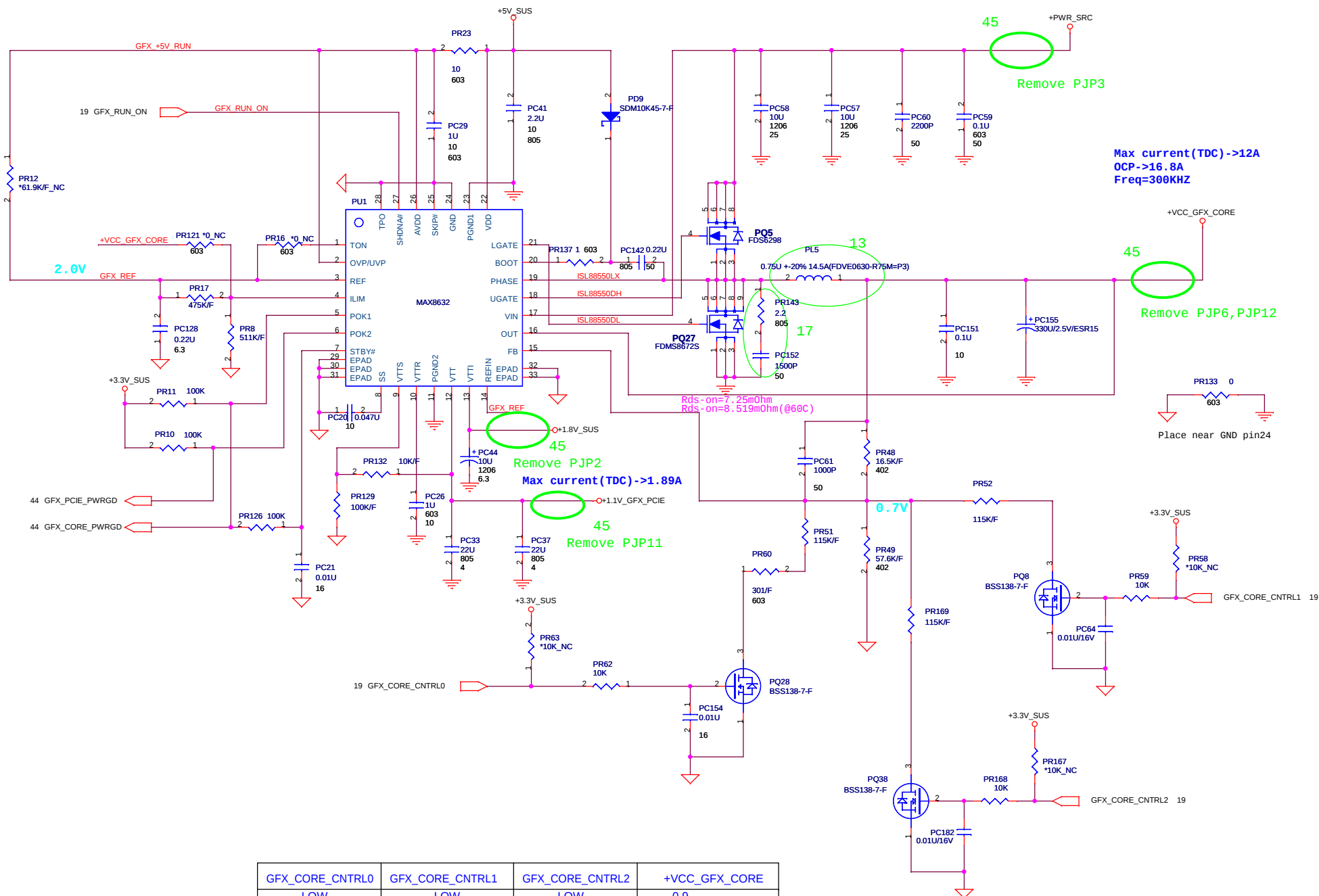
Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

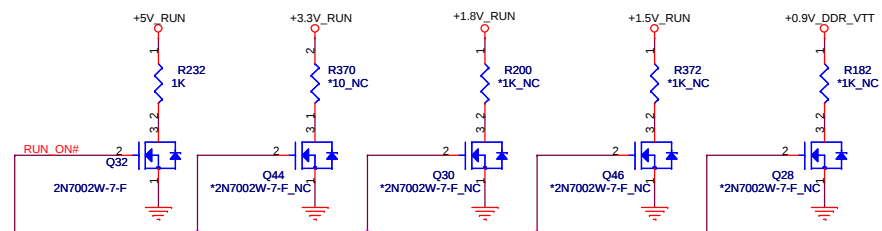
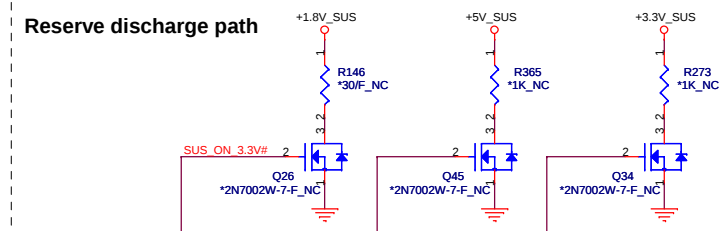
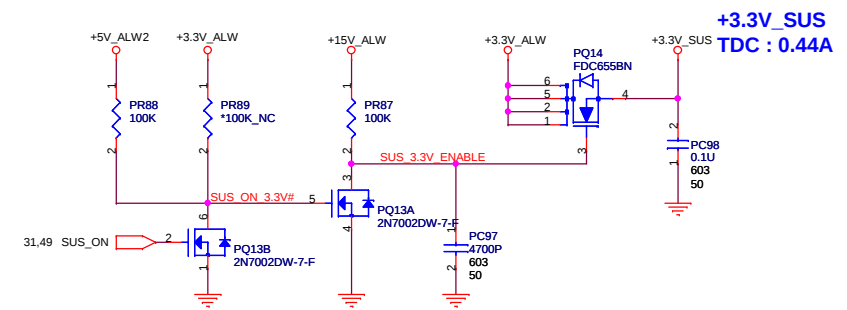
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Title

RUN POWER SW

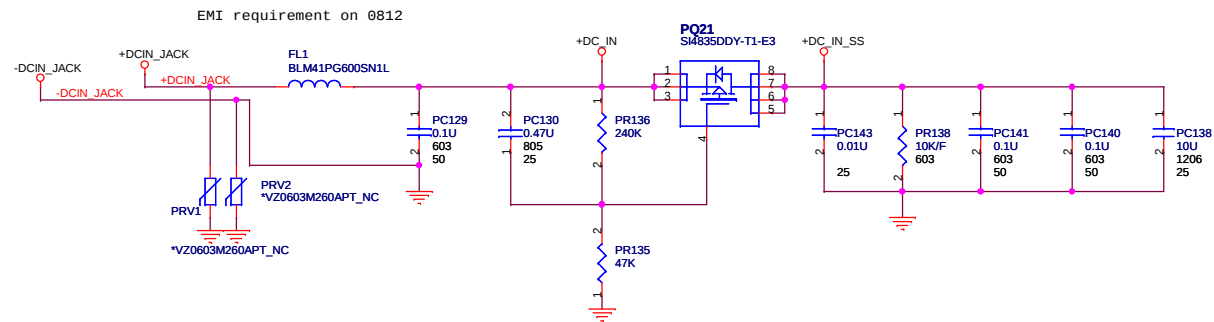
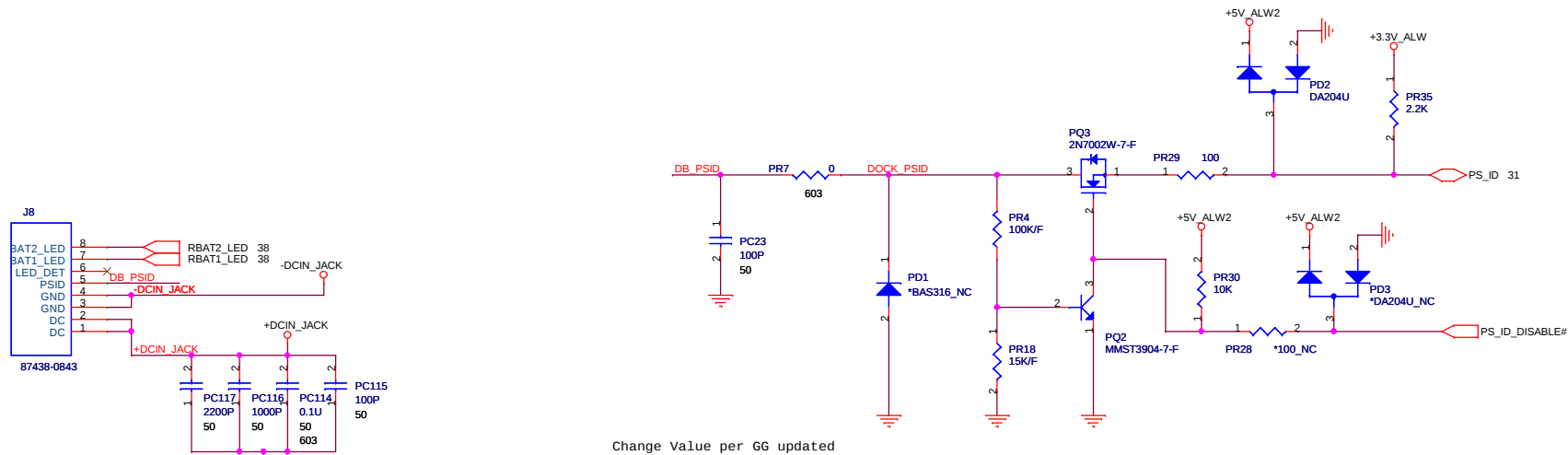
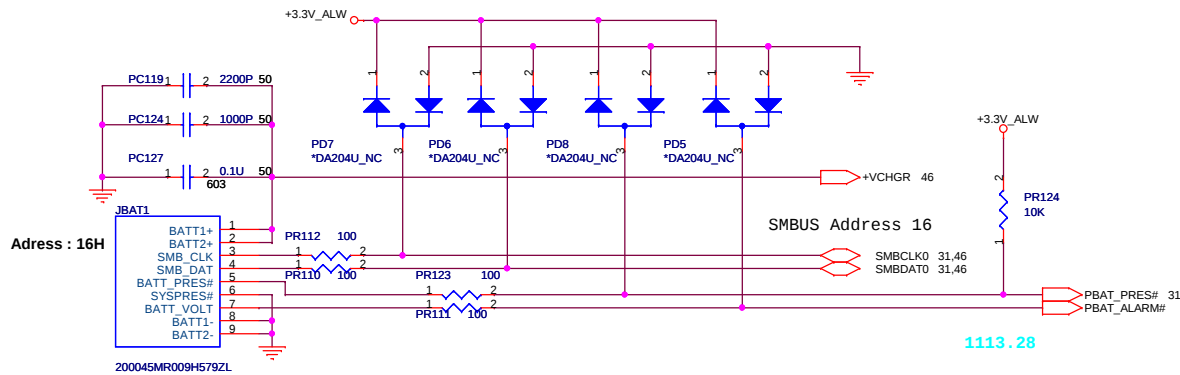
Size

Document Number

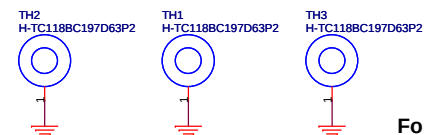
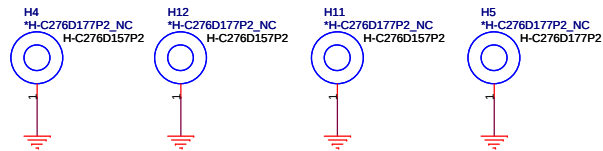
Rev

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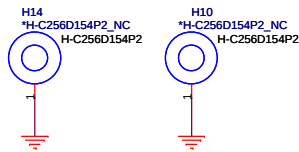
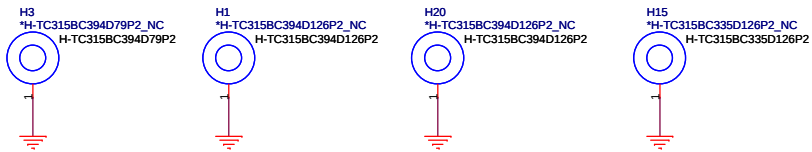
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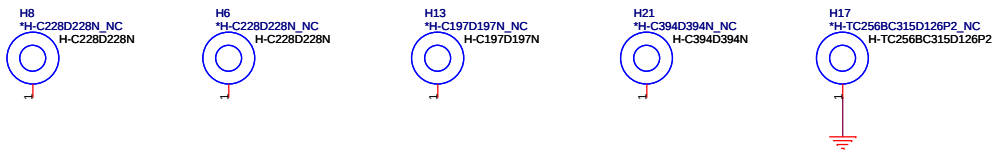
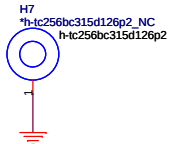
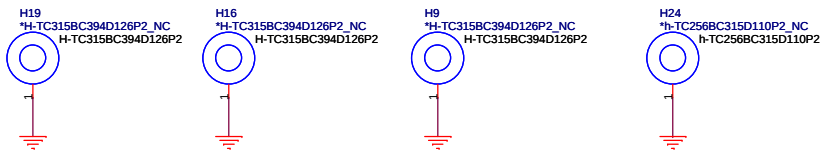
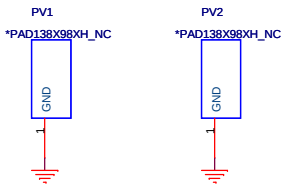
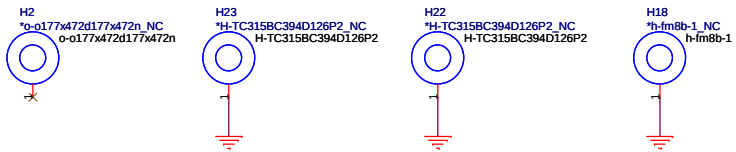
FOR CPU use



For MiniCard nut use.
on 31' header



For GPU nut use.



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Reserved for EMI.



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COMPUTER

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EMI CAP		
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